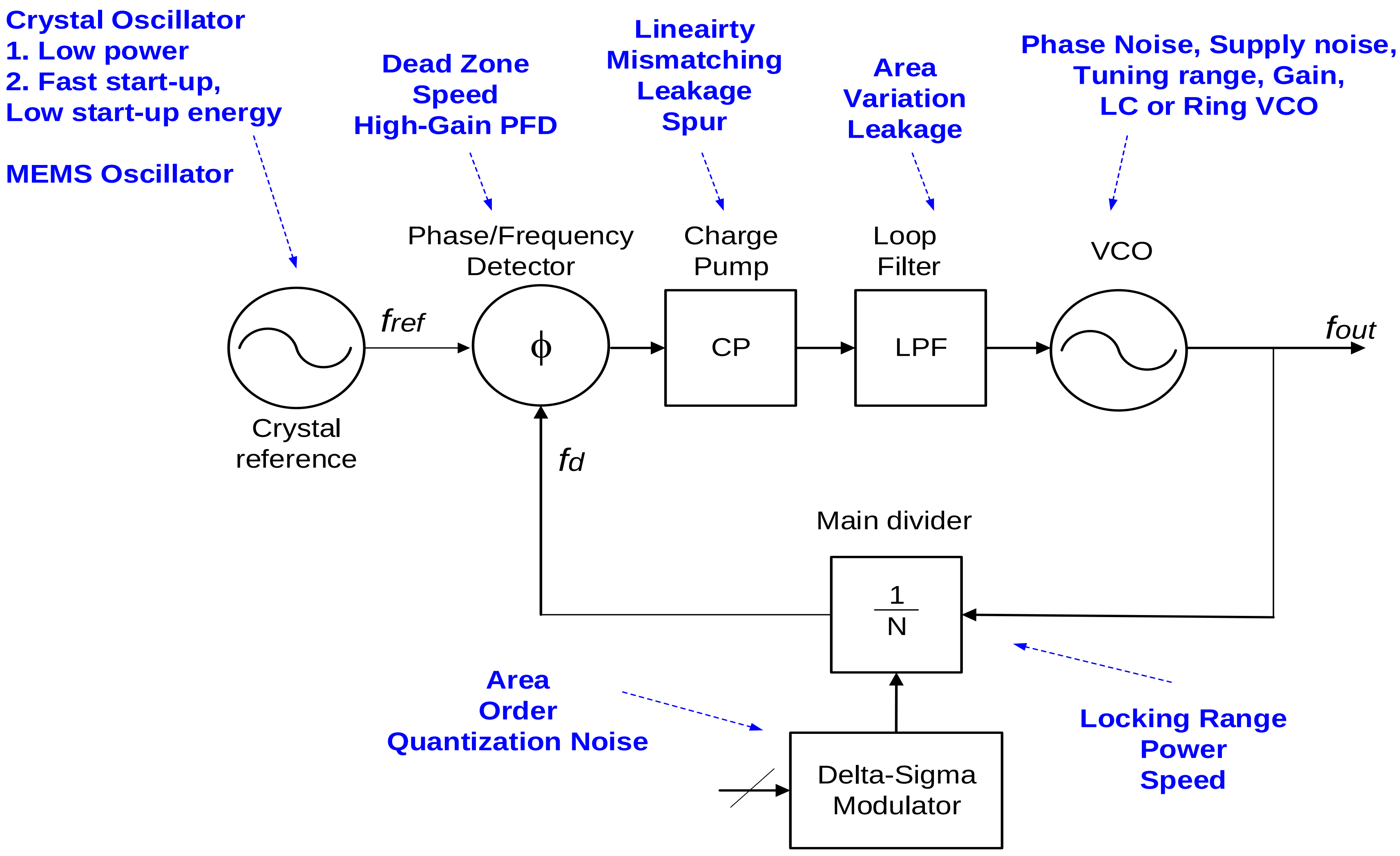
Advanced Phase-Locked Loops

National Taiwan University
Department of Electrical Engineering
& Graduate Institute of Electronics Engineering

Issues in PLLs



Low Noise PLLs

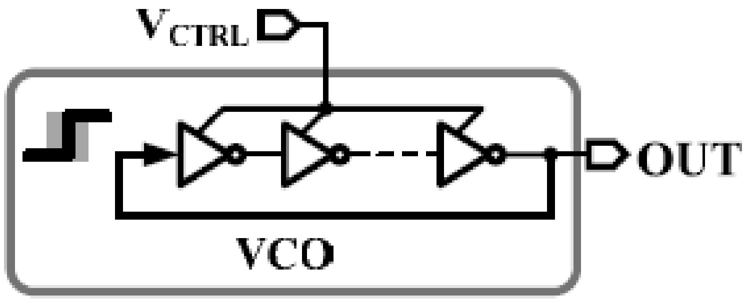
How to reduce the phase noise or jitters of PLLs in SOCs

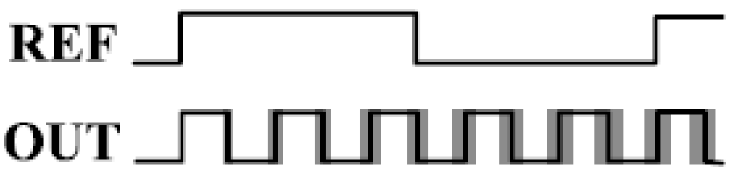
Several solutions

- Multiplying Delay-Locked Loop
- Noise filter: embedded FIR filter
- Sub-harmonically Injection-locked Technique
- Sub-sampling PD
- High-gain PFD
- Dual-Loop Hybrid Architecture

Multiplying Delay-Locked Loop (I)

Ring Oscillator

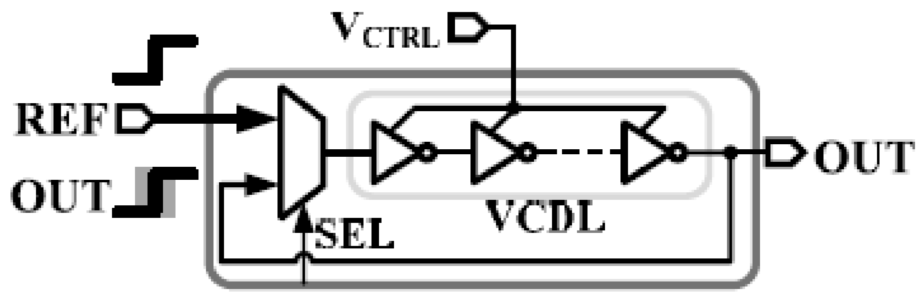


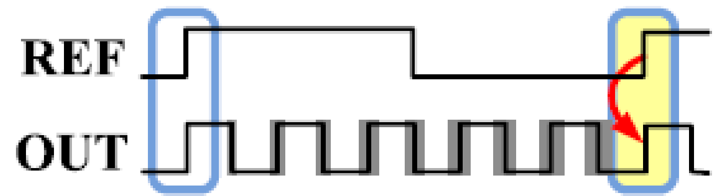


Noise is accumulated

This is at least 2.5 higher than PLLs' highest bandwidth (f_{REF}/10).

MDLL



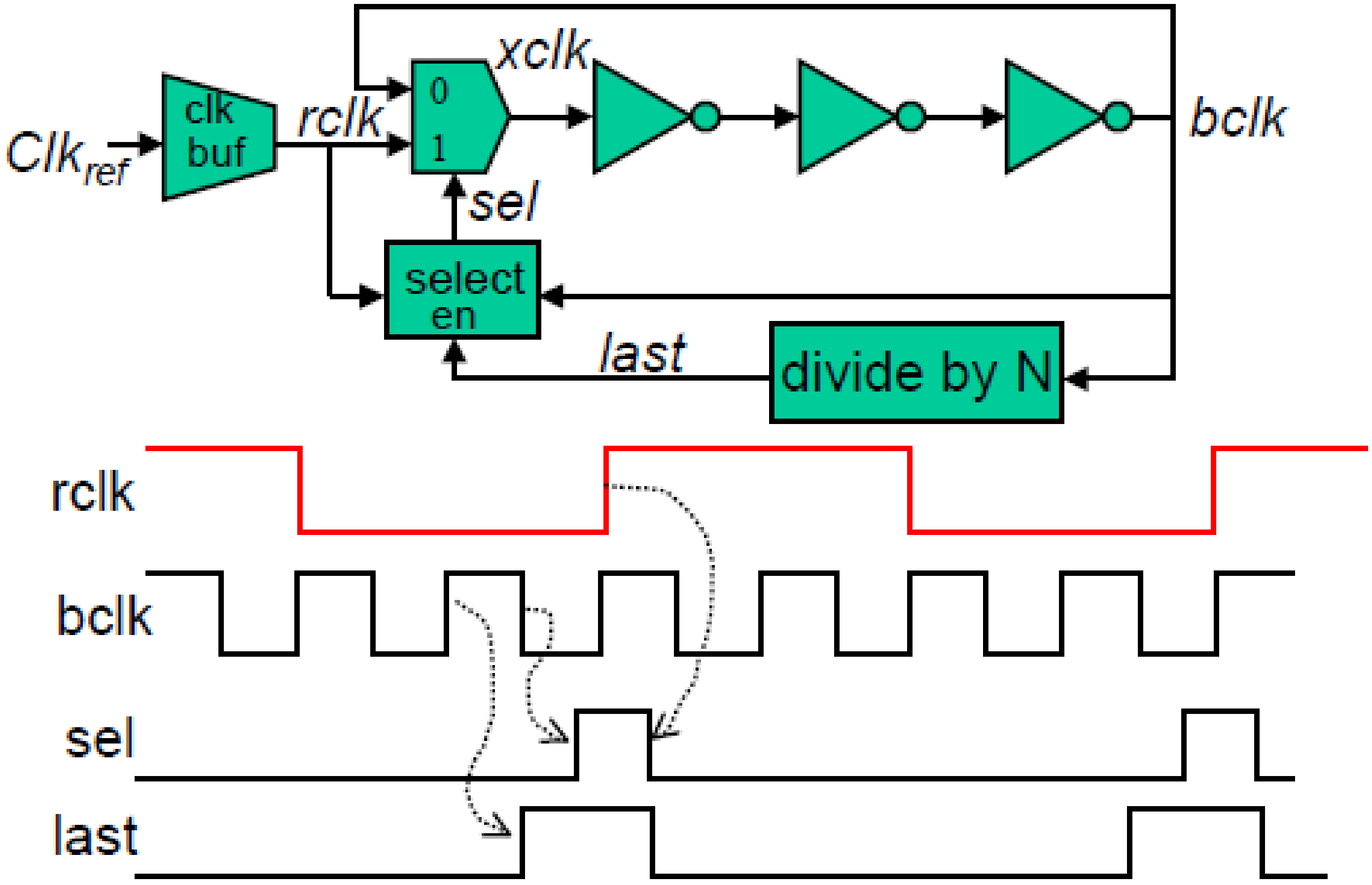


Accumulated Noise reduced

IEEE JSSC, pp. 1416-, June 2013

ISSCC, Feb. 2012

Multiplying Delay-Locked Loop (II)



Recirculating DLL

IEEE JSSC, pp. 1759-, Dec. 2002
IEEE JSSC, pp. 1804-, Dec. 2002
IEEE JSSC, pp. 1222-, Aug. 2004

Low Noise PLLs

Several solutions

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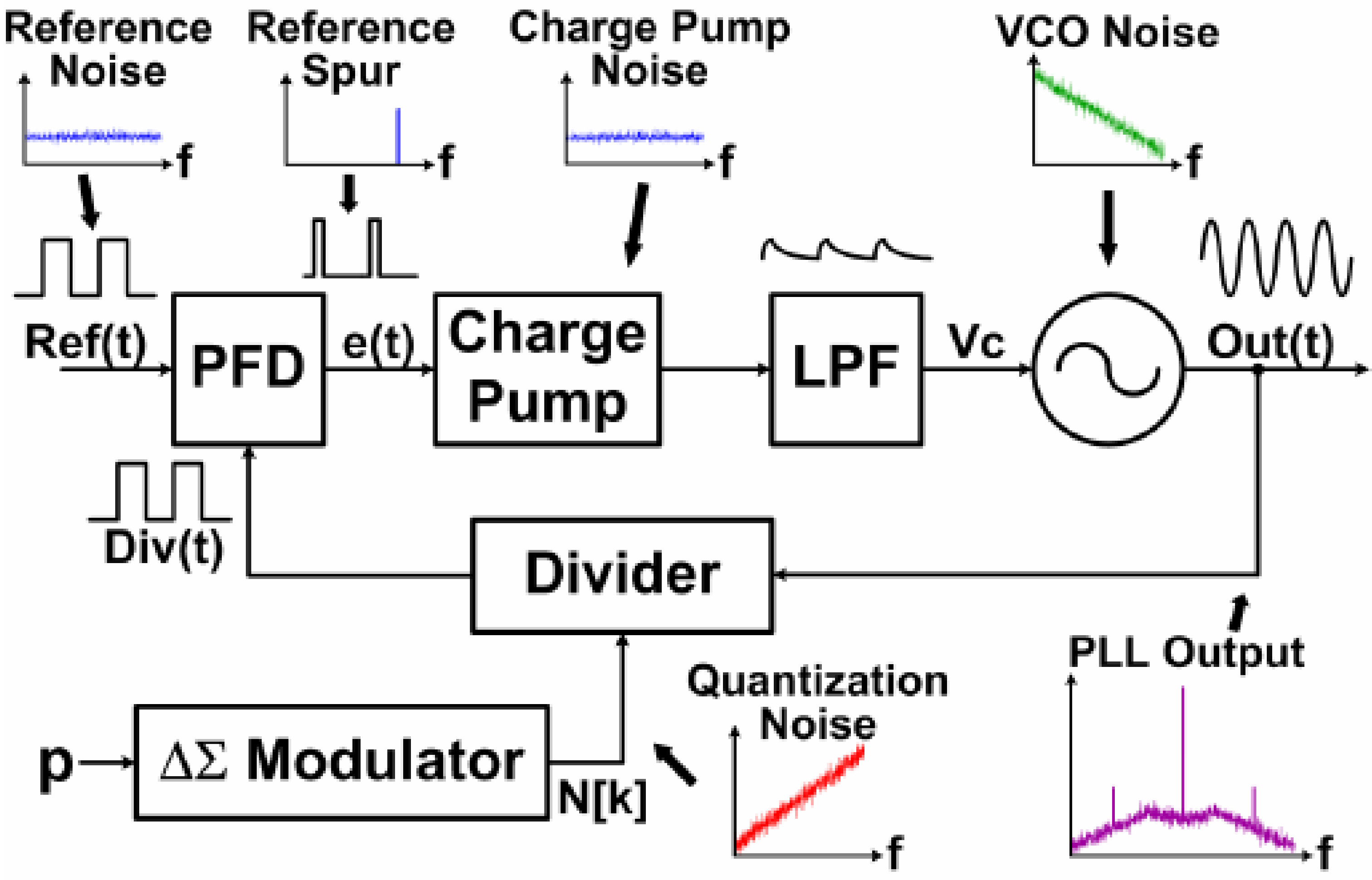
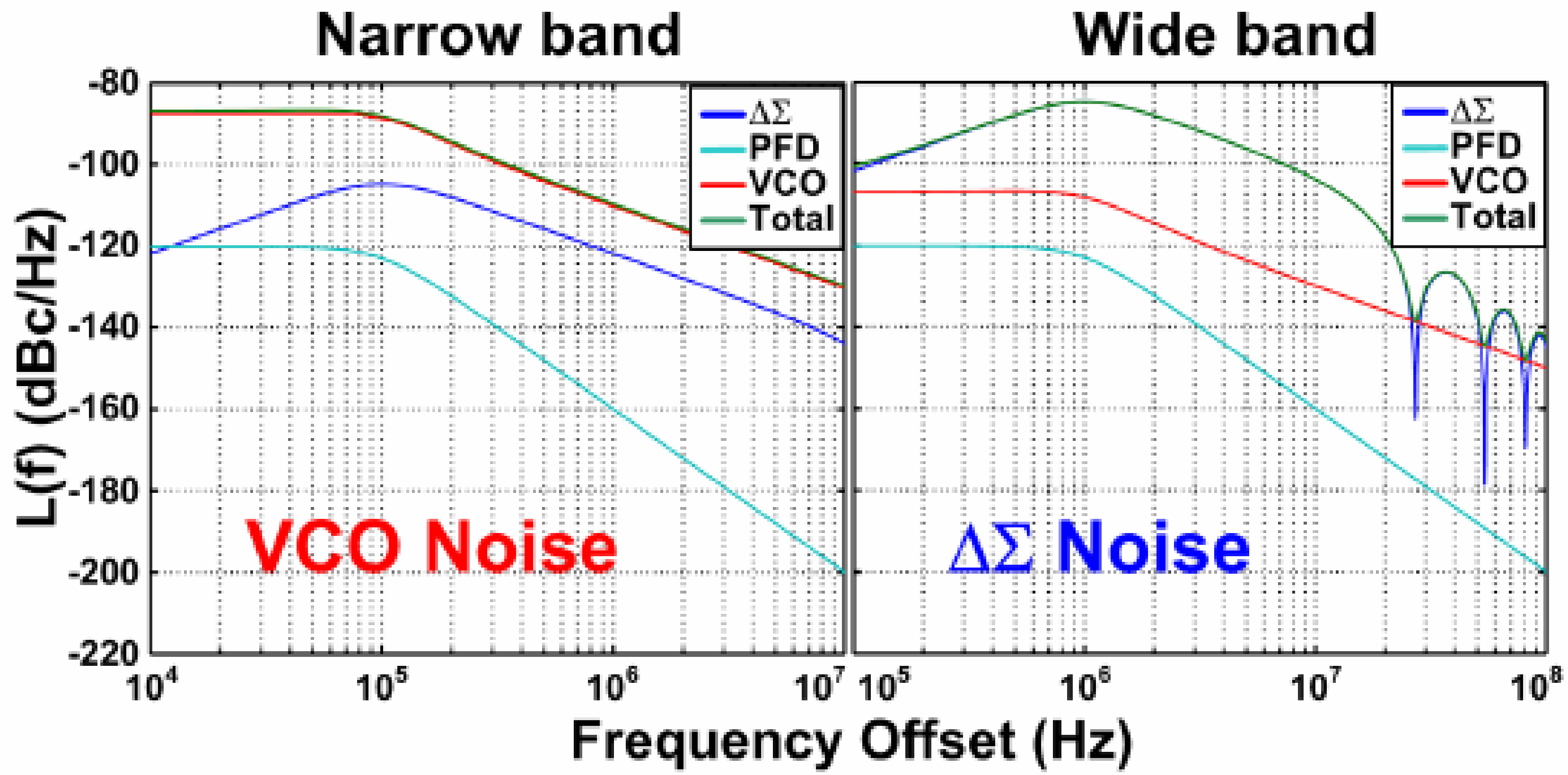
- Sub-harmonically Injection-locked Technique
- Sub-sampling PD
- High-gain PFD
- Dual-Loop Hybrid Architecture

Noises in Fractional-N PLLs



Noises Vs. PLL's Bandwidth

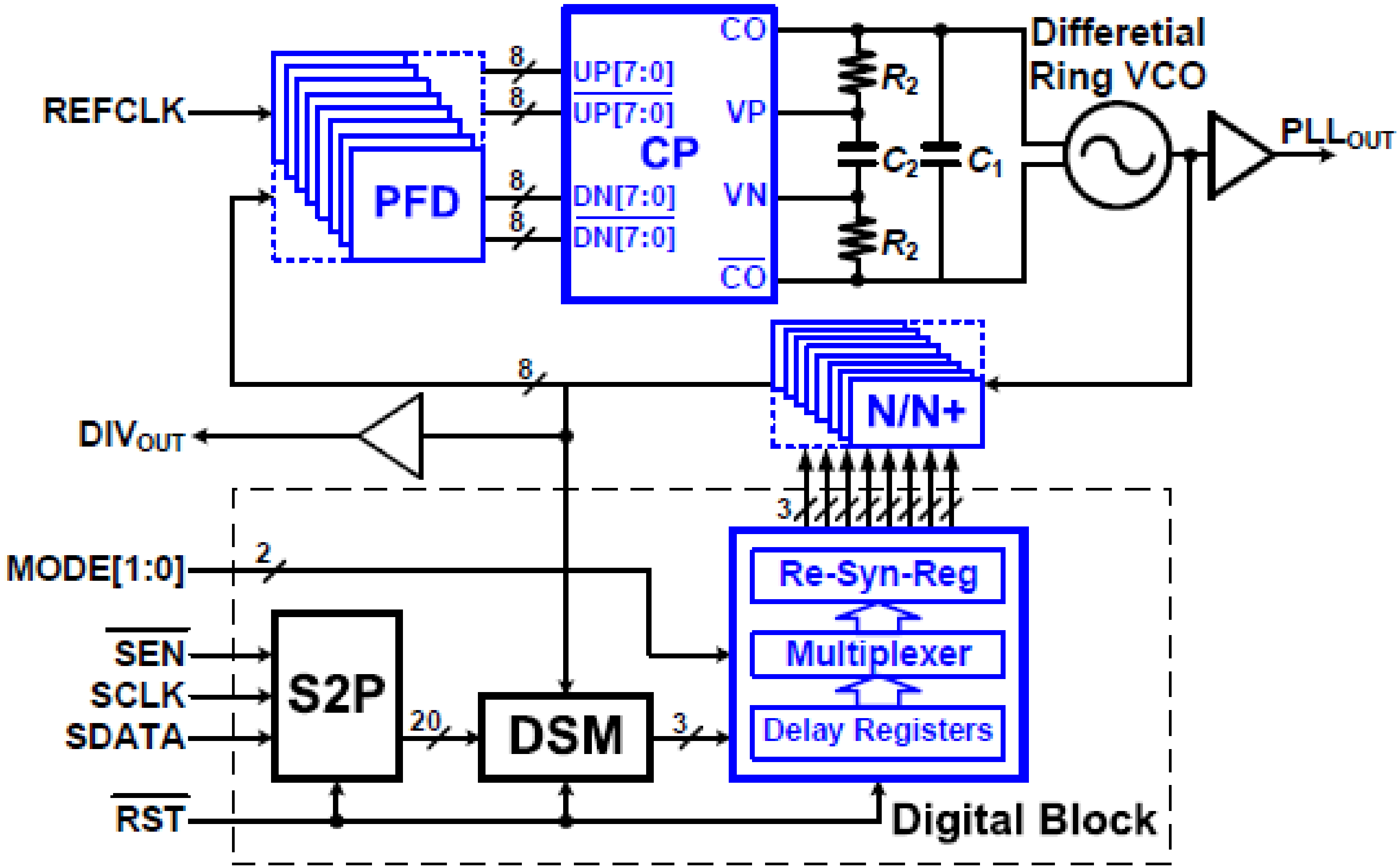


- $OSR_{eff} \sim f_{ref} / (2f_{BW})$

ΔΣ quantization noise will degrade the PN.

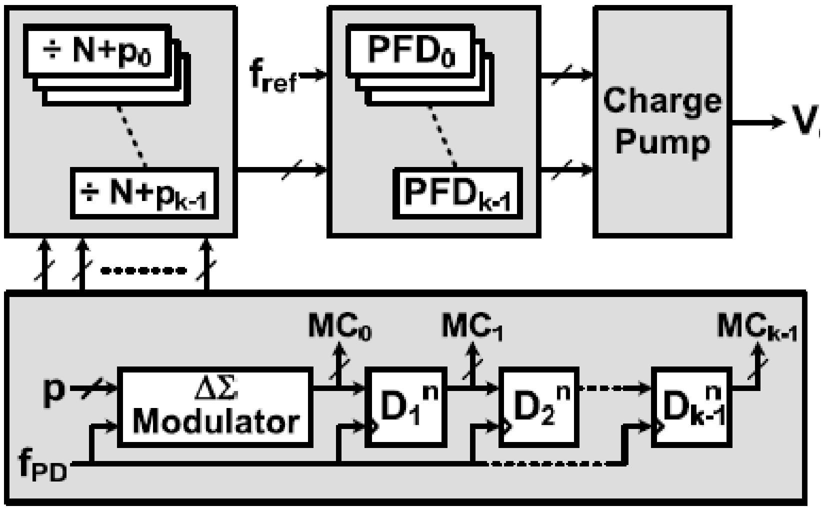
IEEE JSSC, pp. 2426-, Sep. 2009

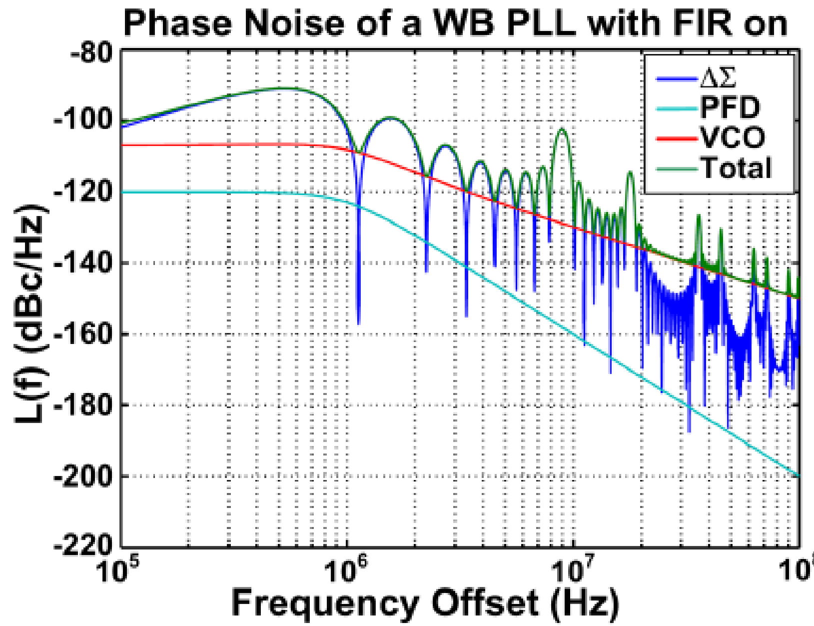
FIR-Embedded Noise Filtering Method

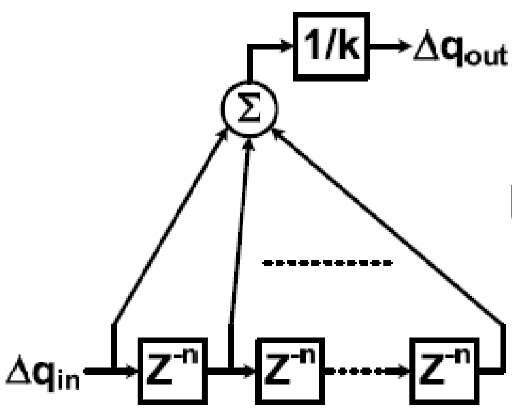


IEEE JSSC, pp. 2426-, Sep. 2009

Noise Filtering in Wideband PLL



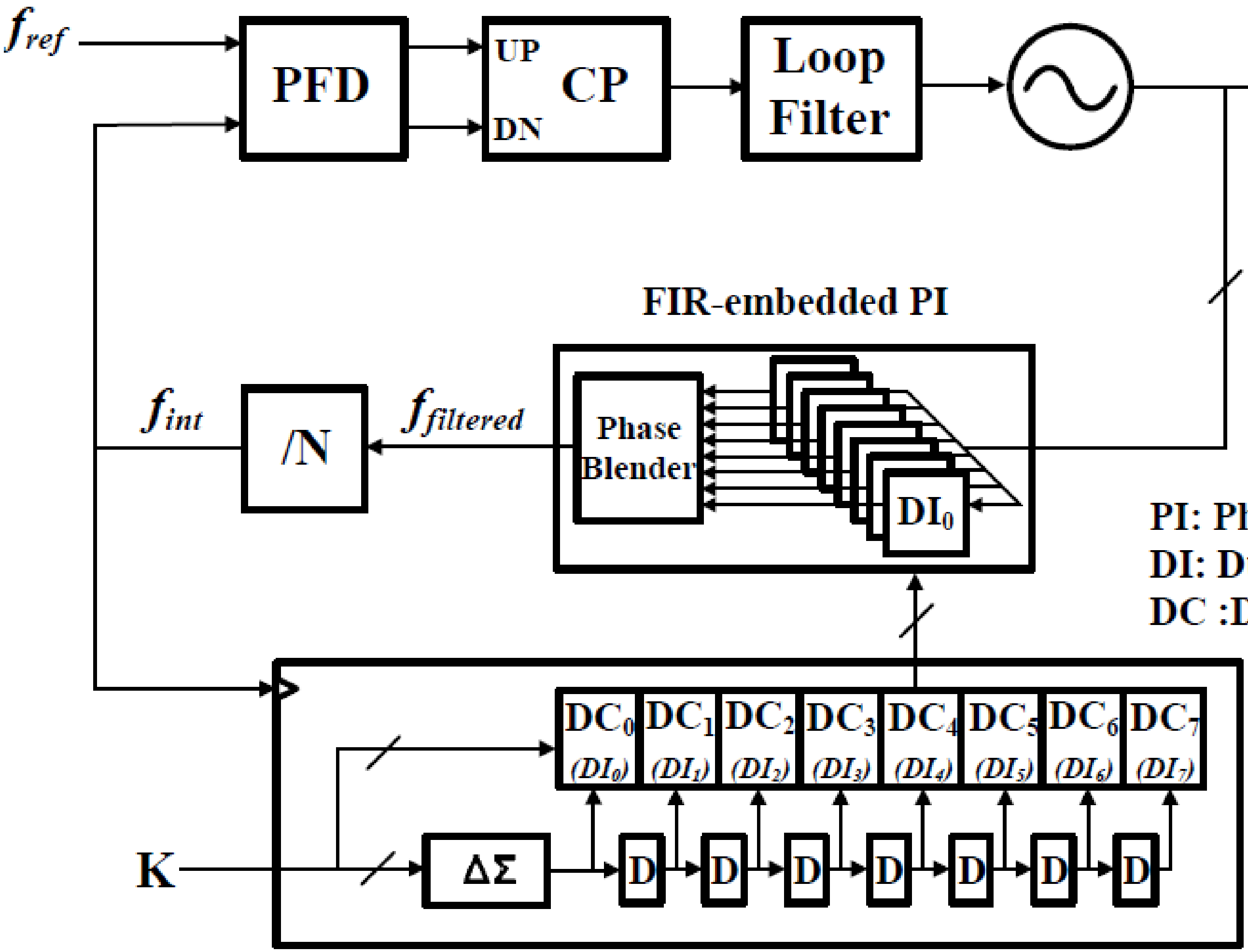




$$H(Z)=(1+Z^{-n}+\ldots+Z^{-(k-1)n})/k$$

$\Delta\Sigma$ quantization noise multiplied by H(z)

PLL with FIR-Embedded Phase Interpolator



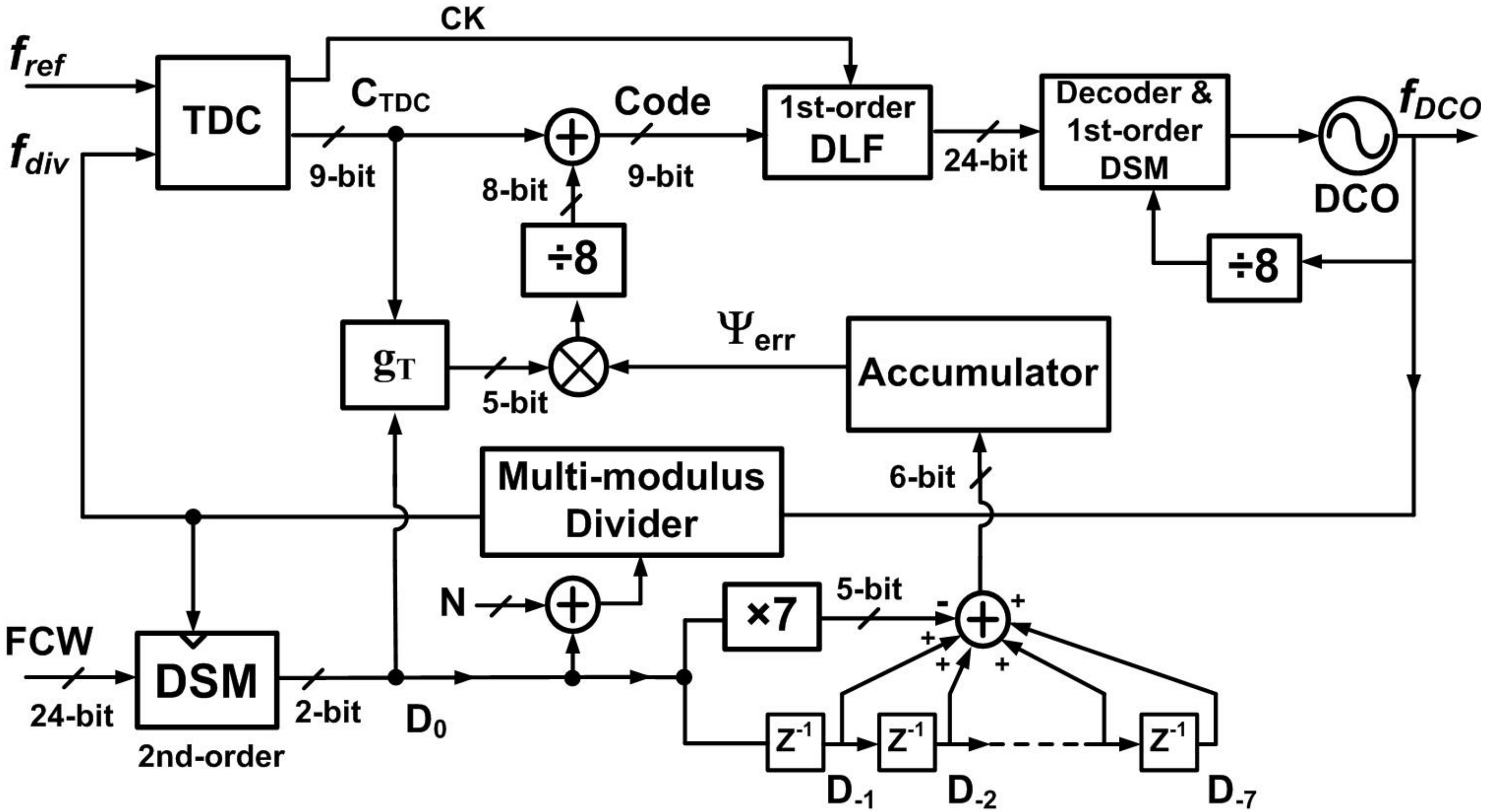
PI: Phase Interpolator
DI: Dual-reference Interpolator
DC :DI controller

ISSCC, Feb. 2011

IEEE JSSC, pp. 2795-, Sep. 2013

$\Delta\Sigma$ quantization noise multiplied by an FIR filter

All-Digital FIR-Embedded Noise Filtering (I)

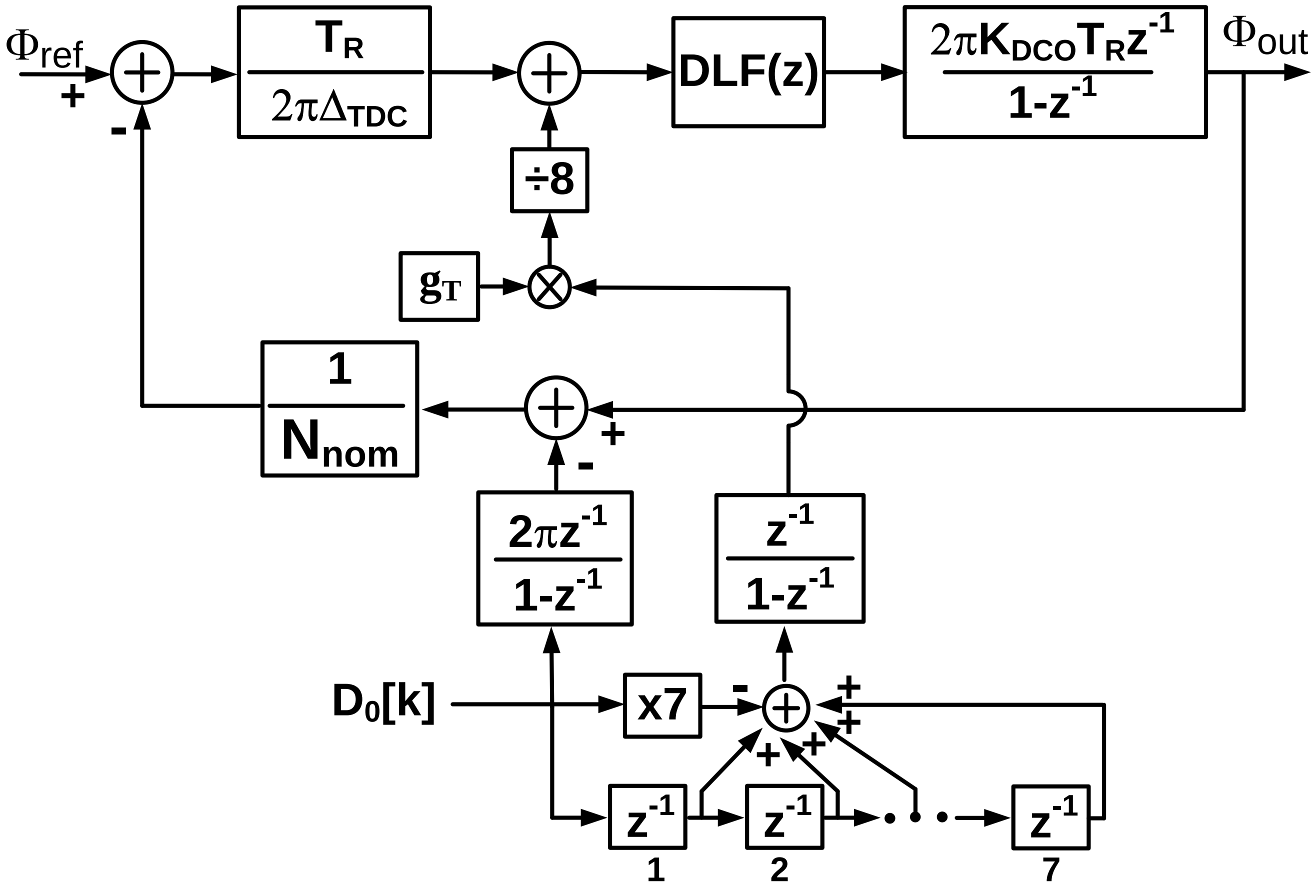


$$D_0[k]\frac{(-7+z^{-1}+z^{-2}+z^{-3}+z^{-4}+z^{-5}+z^{-6}+z^{-7})}{8}+D_0[k]$$

$$=D_0[k]\cdot\frac{(1+z^{-1}+z^{-2}+z^{-3}+z^{-4}+z^{-5}+z^{-6}+z^{-7})}{8}$$

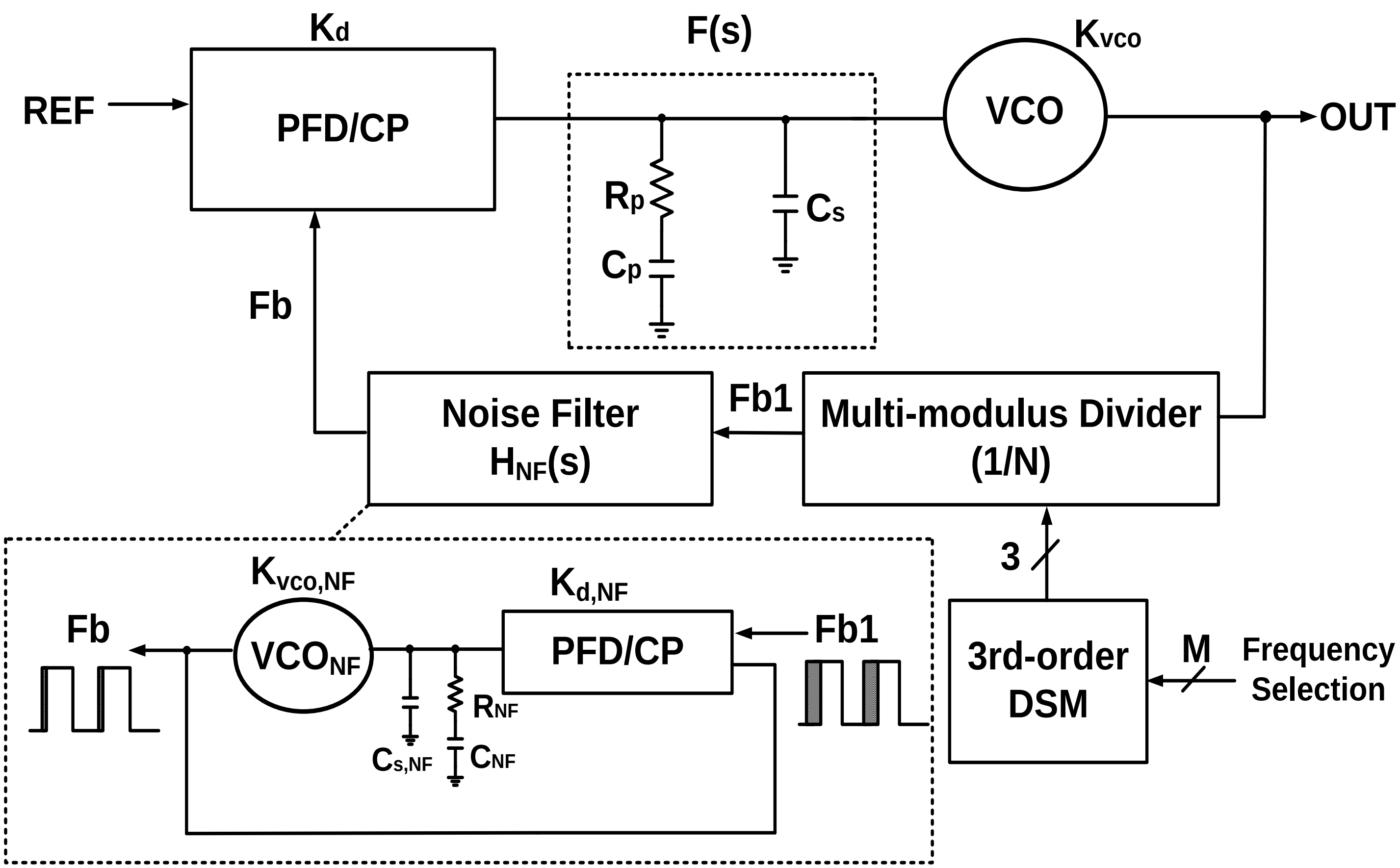
IEEE T-CAS-II, pp. 267-, May 2012

All-Digital FIR-Embedded Noise Filtering (II)



$$\Phi_{out} = \frac{H(z)}{1+H(z)} \cdot D_0[k] \cdot \frac{2\pi z^{-1}}{1-z^{-1}} \cdot \frac{1}{8}(1+z^{-1}+z^{-2}+z^{-3}+z^{-4}+z^{-5}+z^{-6}+z^{-7})$$

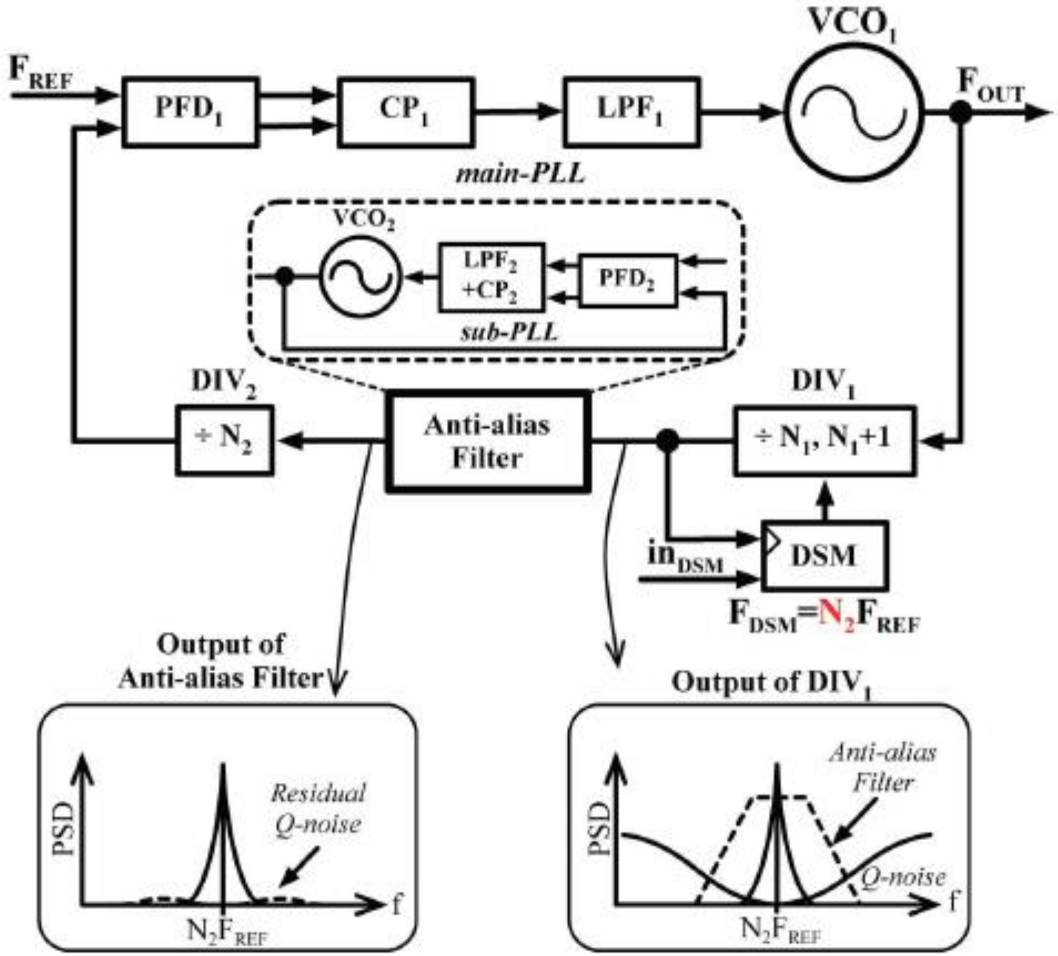
Fractional-N PLL with a Noise Filter



$\Delta\Sigma$ quantization noise multiplied by $H_{NF}(s)$

IEEE T-CAS-II, pp. 139-, March 2011

Fractional-N PLL with a Nested PLL



- **Feedback divider is split to increase the operating frequency of the DSM**
- **Suppress quantization noise**

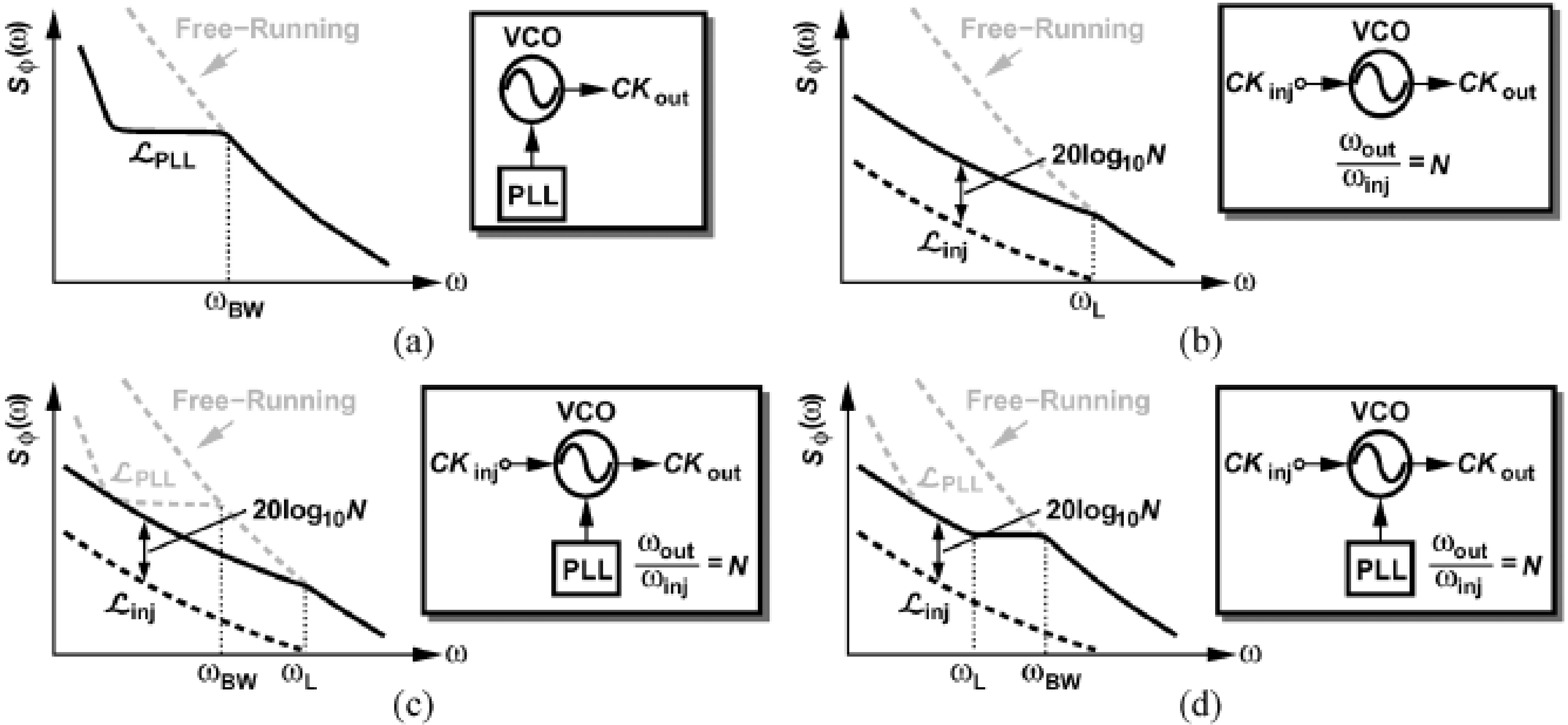
IEEE JSSC, pp. 2433-, Oct. 2012

Low Noise PLLs

Several solutions

- Multiplying Delay-Locked Loop
- Noise filter: embedded FIR filter
- Sub-harmonically Injection-locked Technique
- Sub-sampling PD
- High-gain PFD
- Dual-Loop Hybrid Architecture

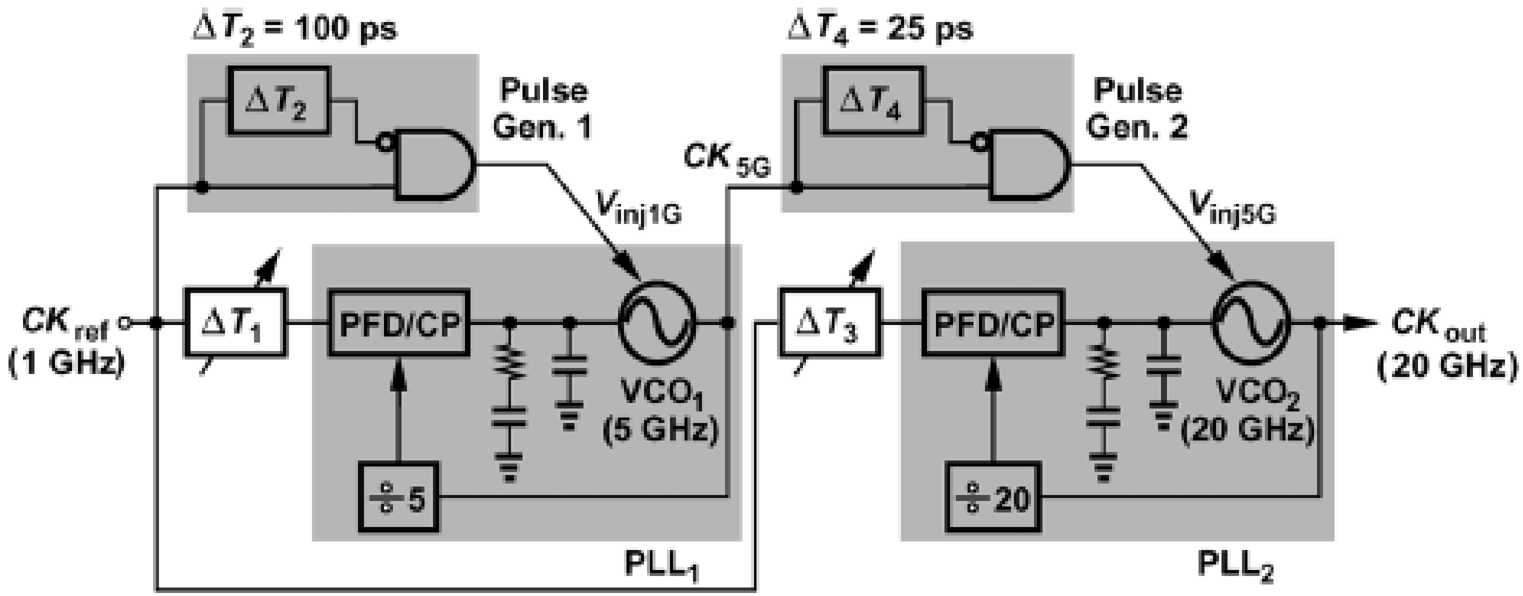
Sub-harmonically Injection-Locked Technique



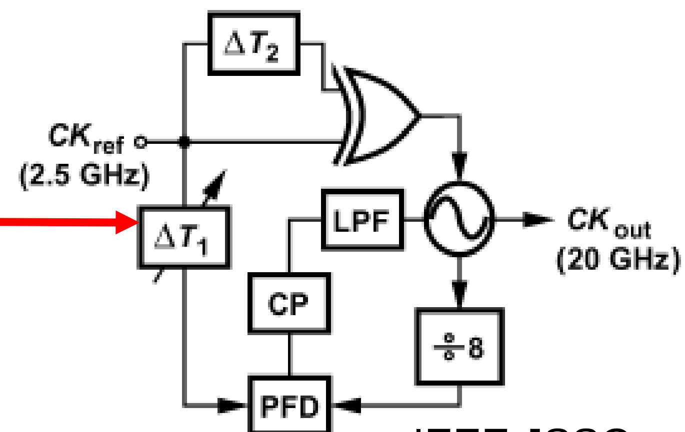
Realigned PLL

IEEE JSSC, pp. 1759-, Dec. 2002
IEEE JSSC, pp. 1539-, May 2009
IEEE TCAS-I, pp. 355-, Jan. 2019

Sub-harmonically Injection-Locked PLLs

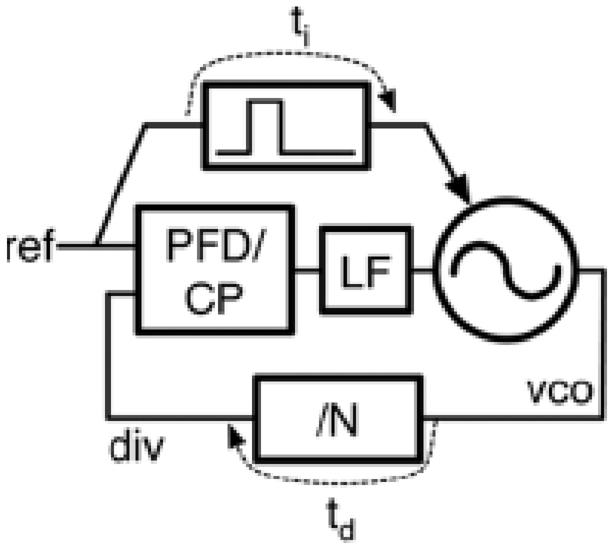


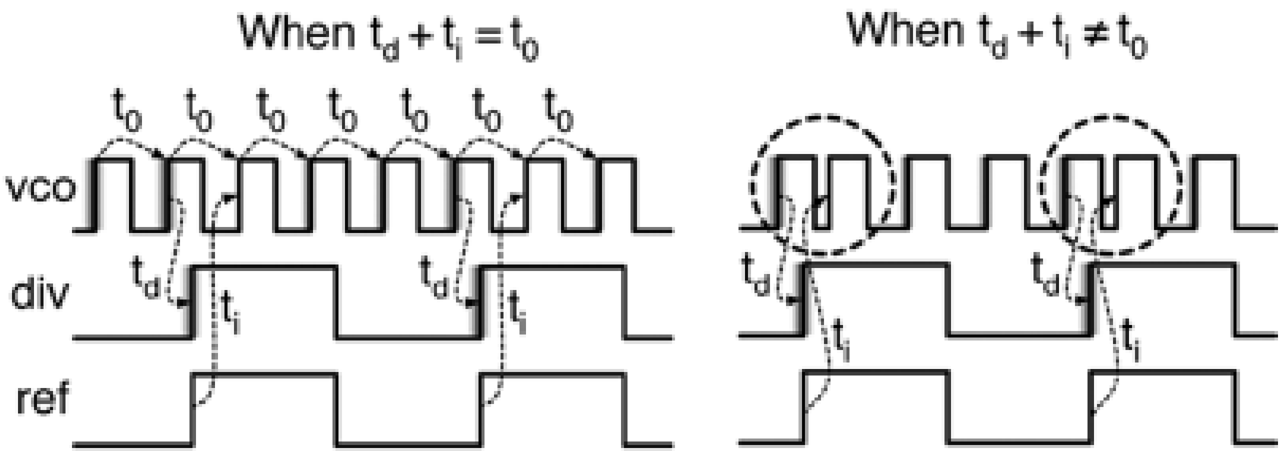
Can it be automatically controlled?



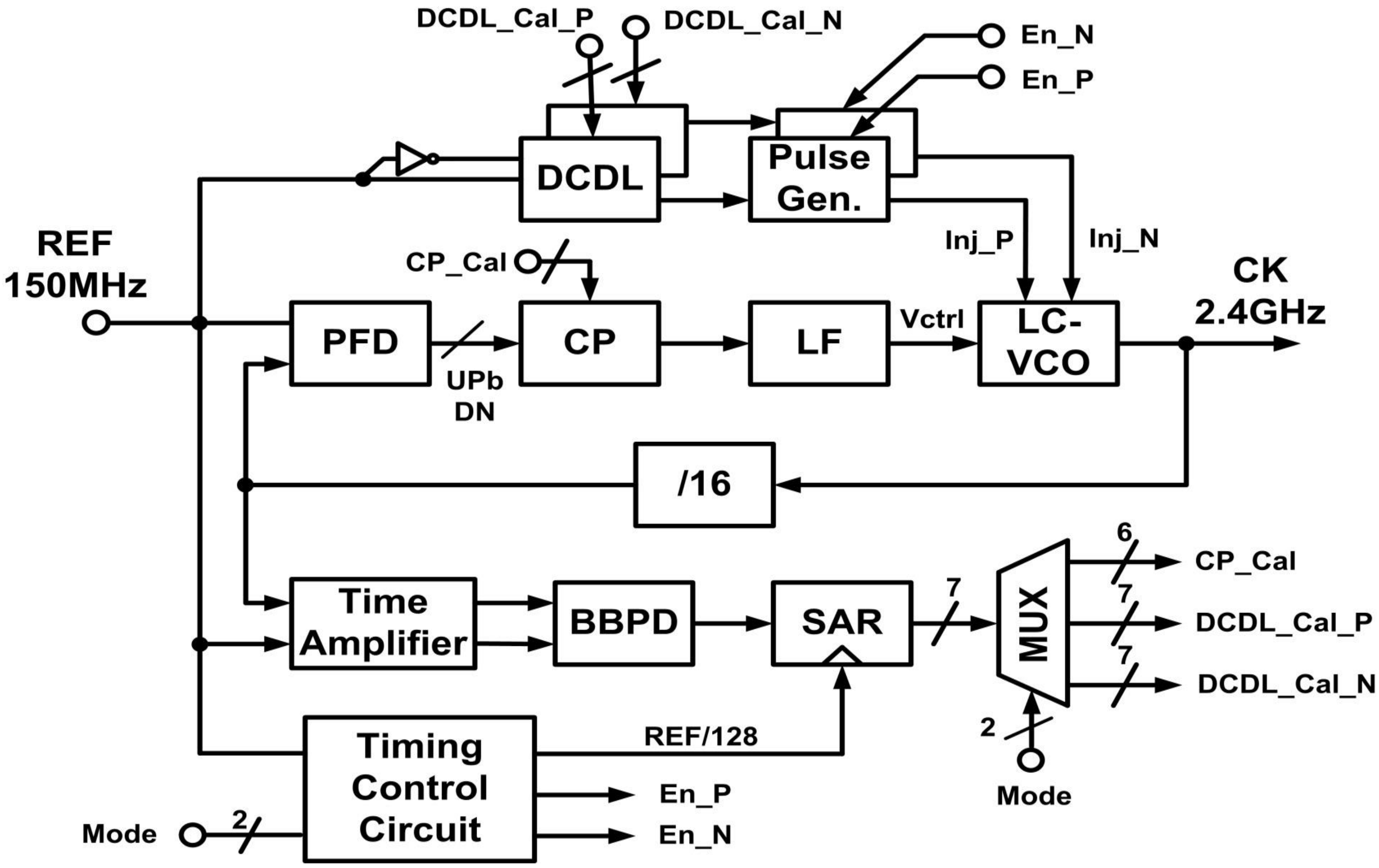
IEEE JSSC, pp. 1539-, May 2009

Injection Timing Issue





A PLL with Self-Calibrated Injection Timing

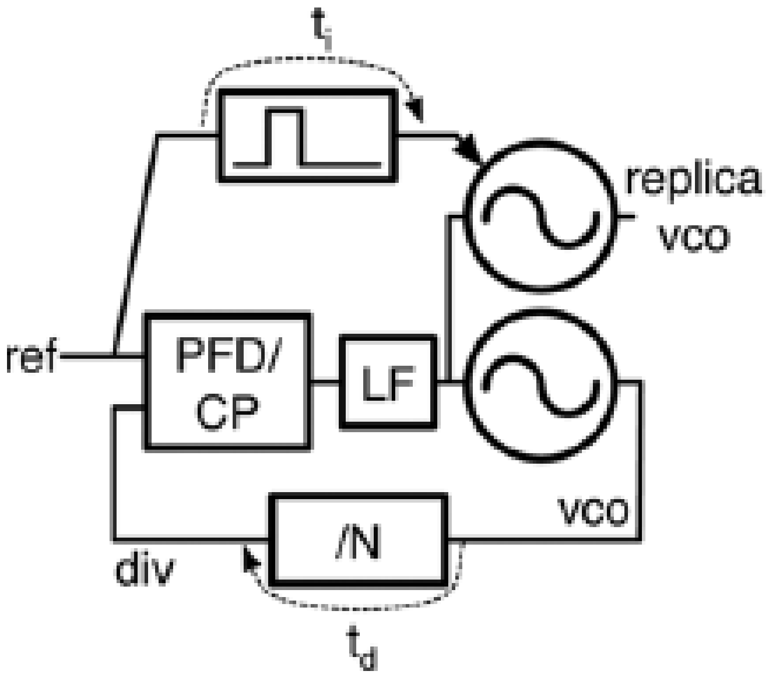


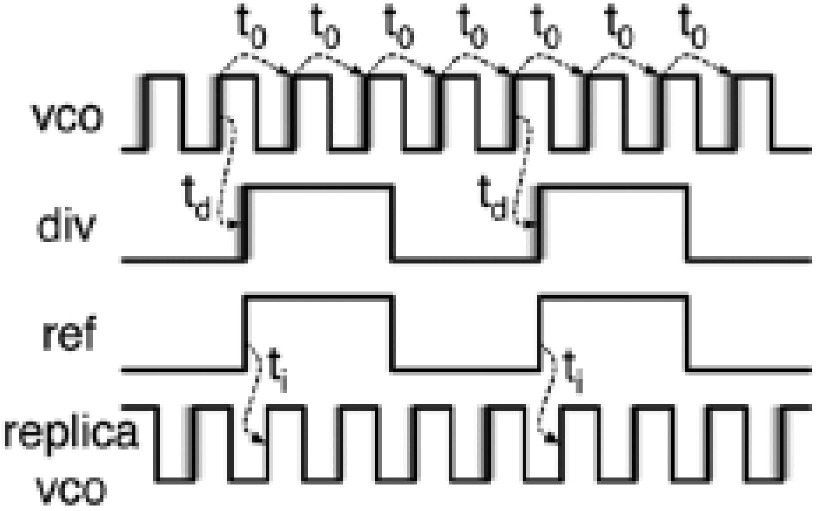
- Calibrate the CP current mismatch to educe the static phase error
- Calibrate the injection timing to tolerate the process variations

IEEE JSSC, pp. 417-, Feb. 2013

Replica VCO

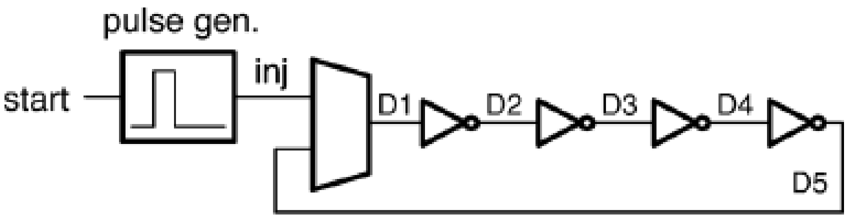
To suppress the reference spur



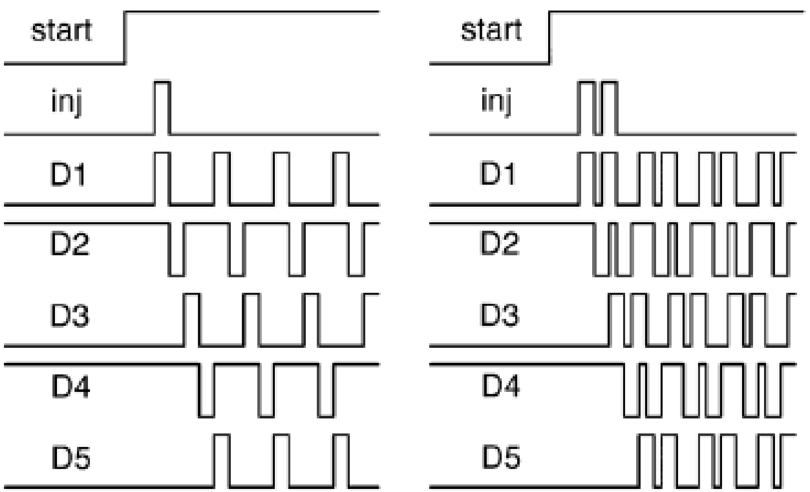


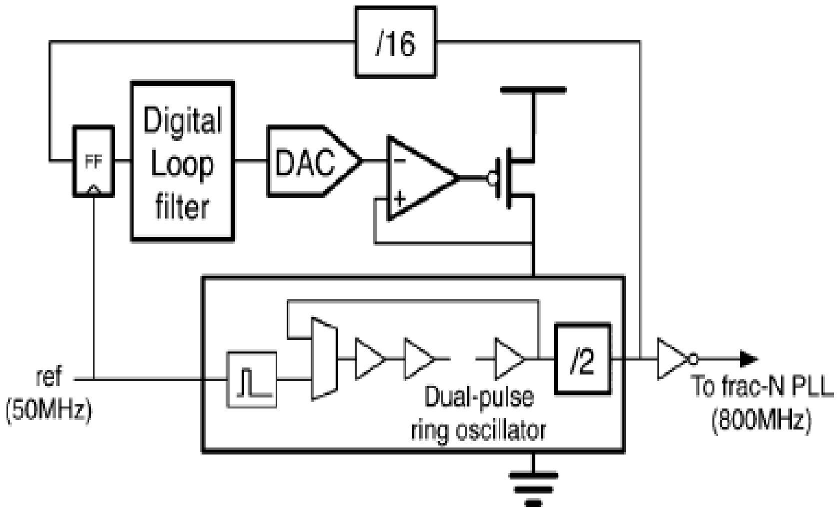
IEEE JSSC, pp. 2989-, Dec. 2012

Dual-Pulse Ring Oscillator (DPRO) (I)



(a)

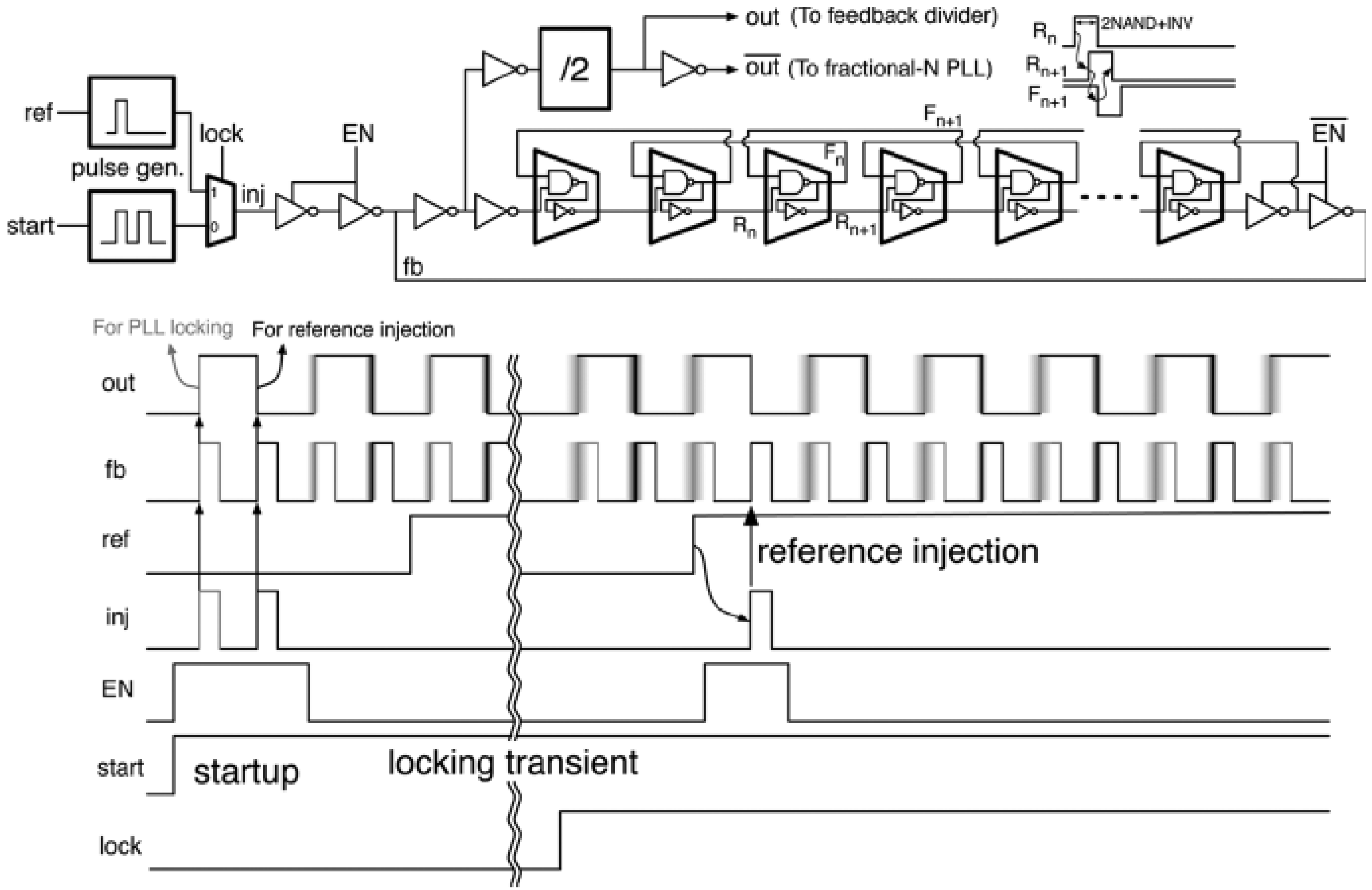




Even inverters --> the loop will not oscillate

DPRO is considered as perfect replica VCOs

Dual-Pulse Ring Oscillator (DPRO) (II)



IEEE JSSC, pp. 2989-, Dec. 2012

Low Noise PLLs

Several solutions

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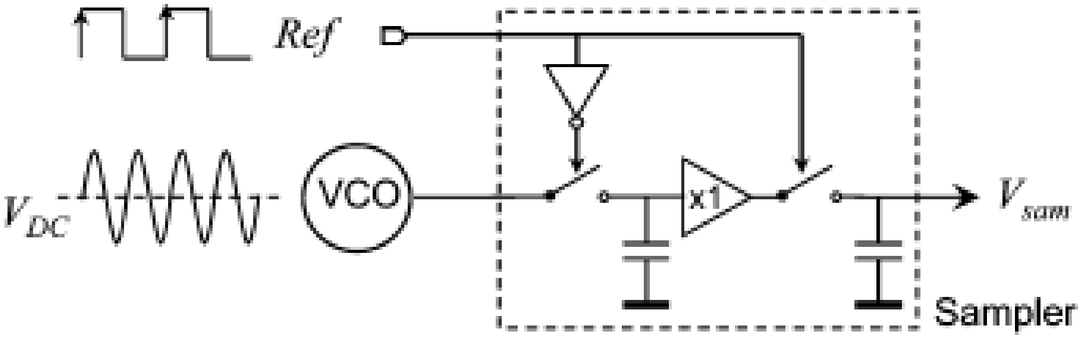
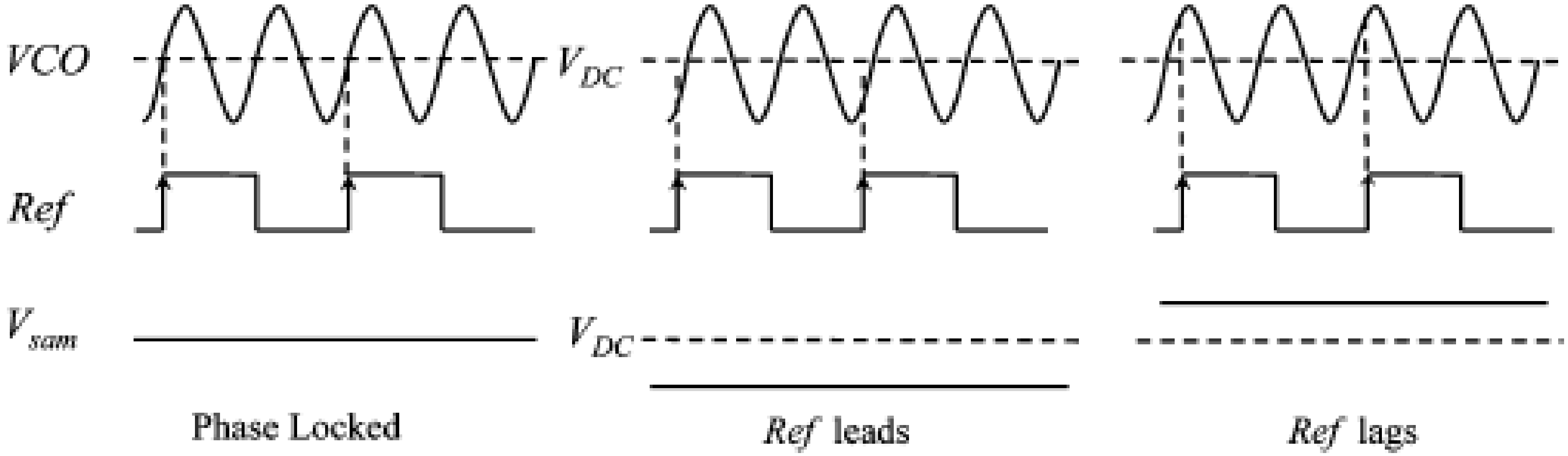
Conceptual Sub-Sampling PD



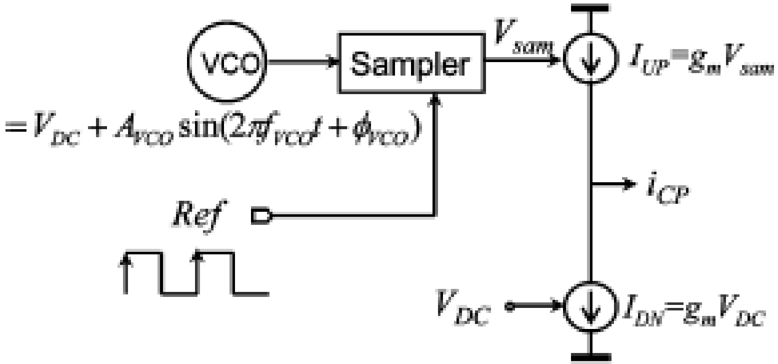
(a)

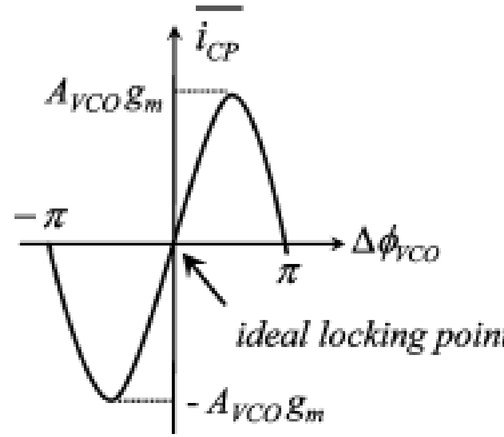


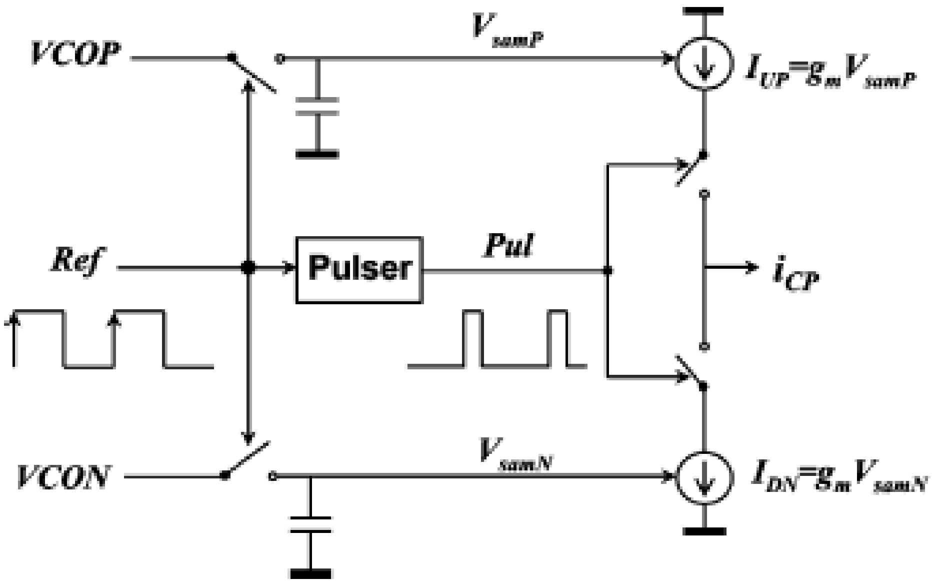
(b)

IEEE JSSC, pp. 3253-, Dec. 2009

High-Gain Sub-Sampling PD

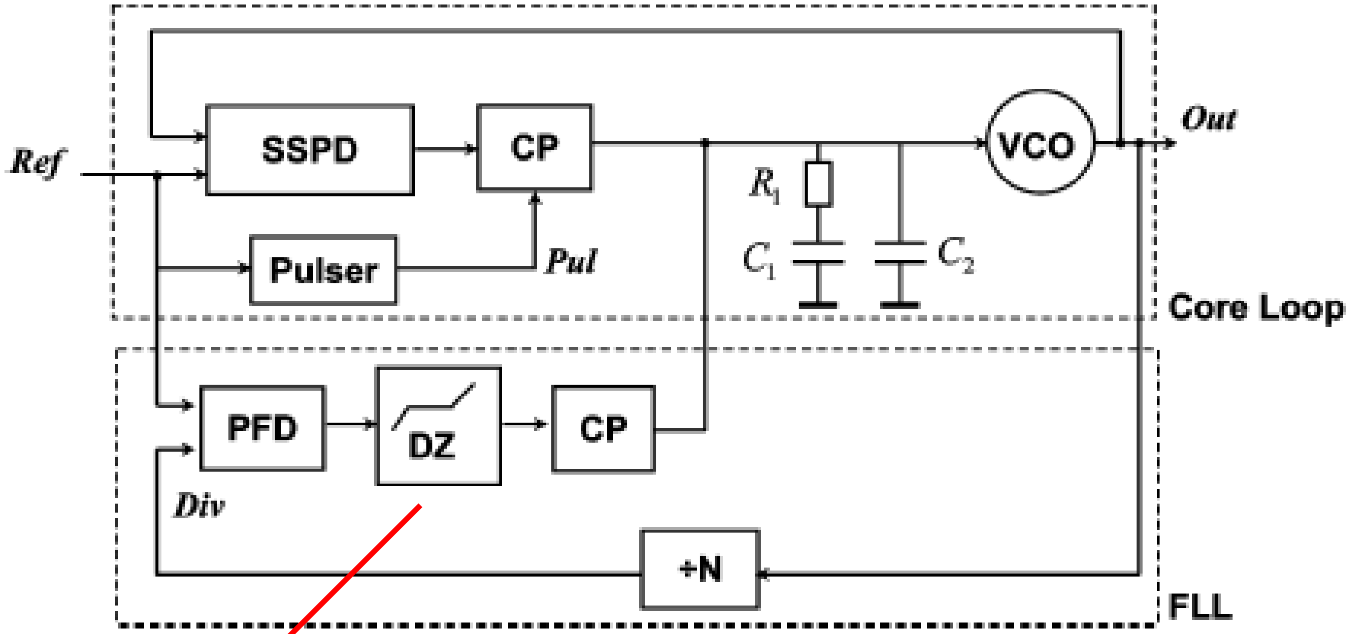


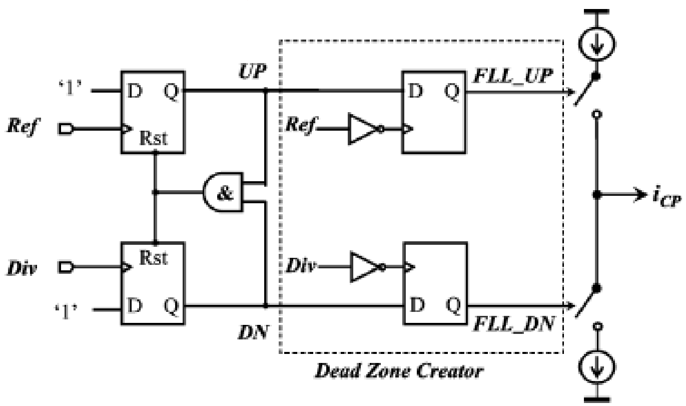




IEEE JSSC, pp. 3253-, Dec. 2009

A PLL Using A Sub-Sampling PD



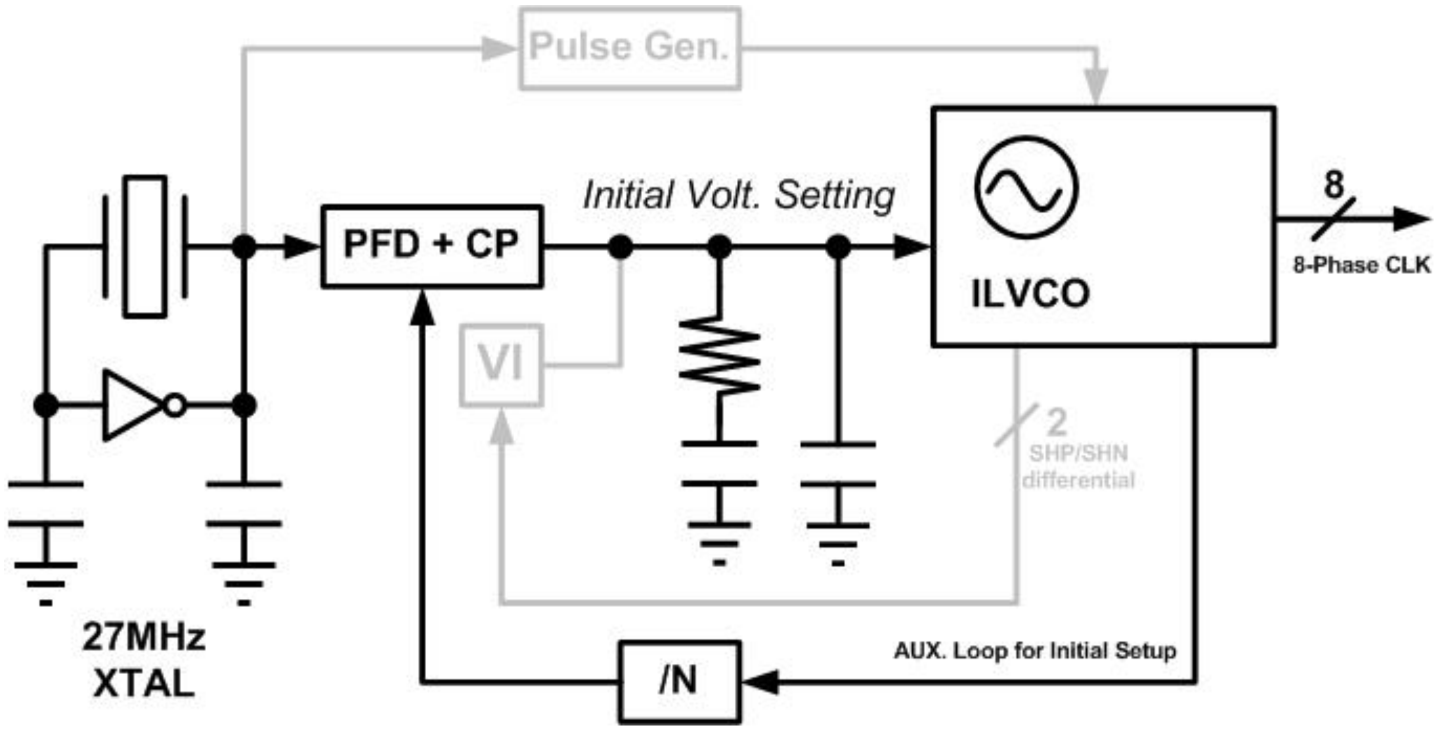


Why low noise?

1. Dividerless in Locking
2. High-Gain PD

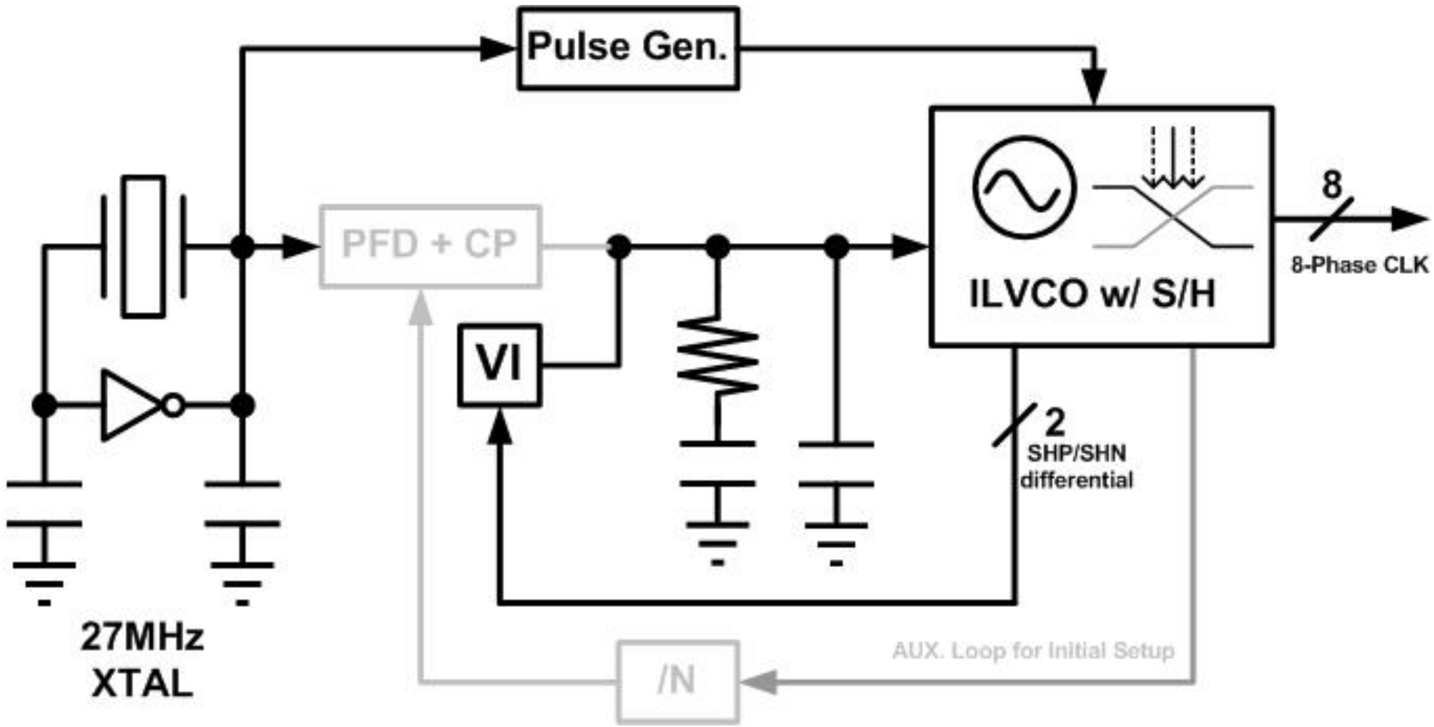
IEEE JSSC, pp. 3253-, Dec. 2009

An Injection-Locked PLL with Self-Aligned Injection (I)



ISSCC, pp.90-91, Feb. 2011

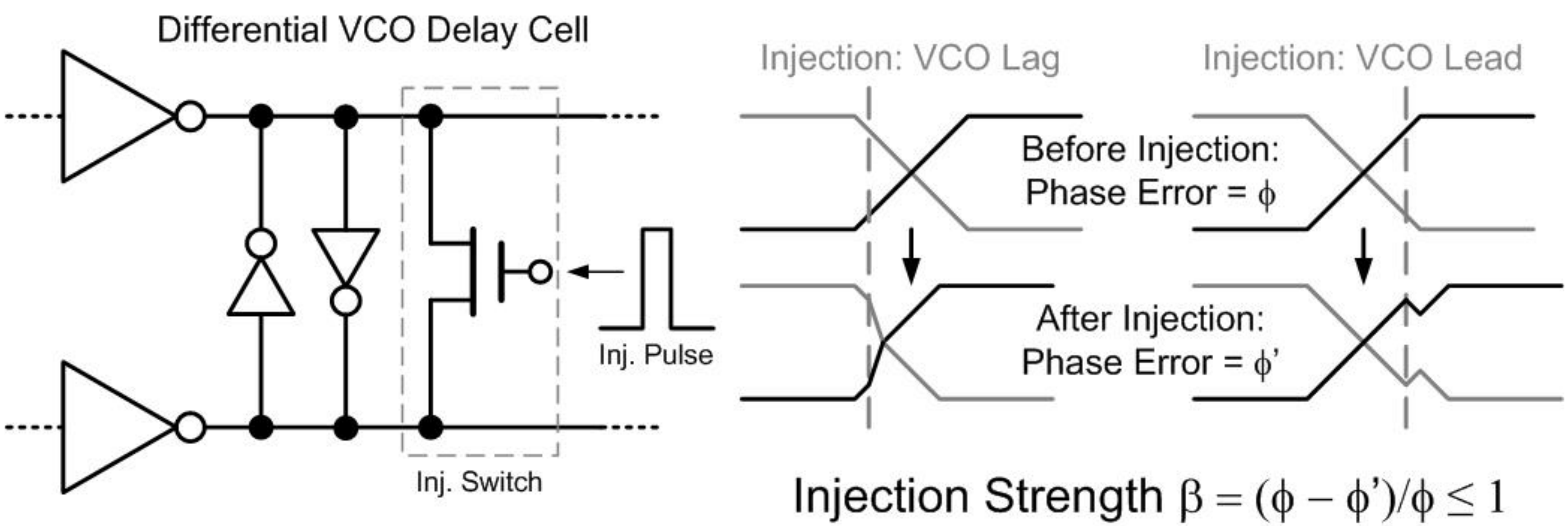
An Injection-Locked PLL with Self-Aligned Injection (II)



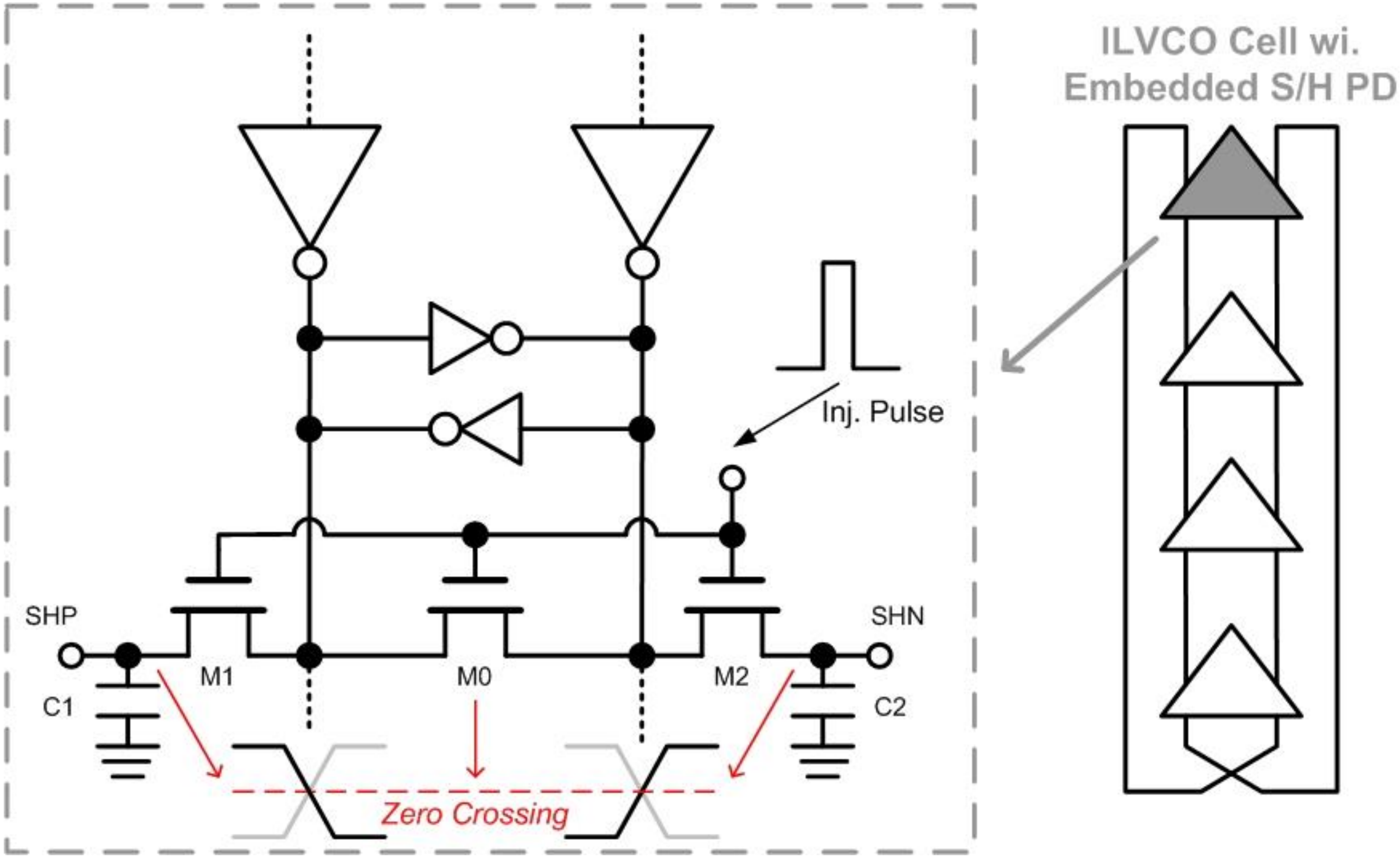
ISSCC, pp.90-91, Feb. 2011

An Injection-Locked PLL with Self-Aligned Injection (III)

- Selected VCO architecture for injection
- Defining β as the injection strength
  - $0.83 < \beta < 0.91$ in this work



Injection-Locked VCO with S/H PD



ISSCC, pp.90-91, Feb. 2011

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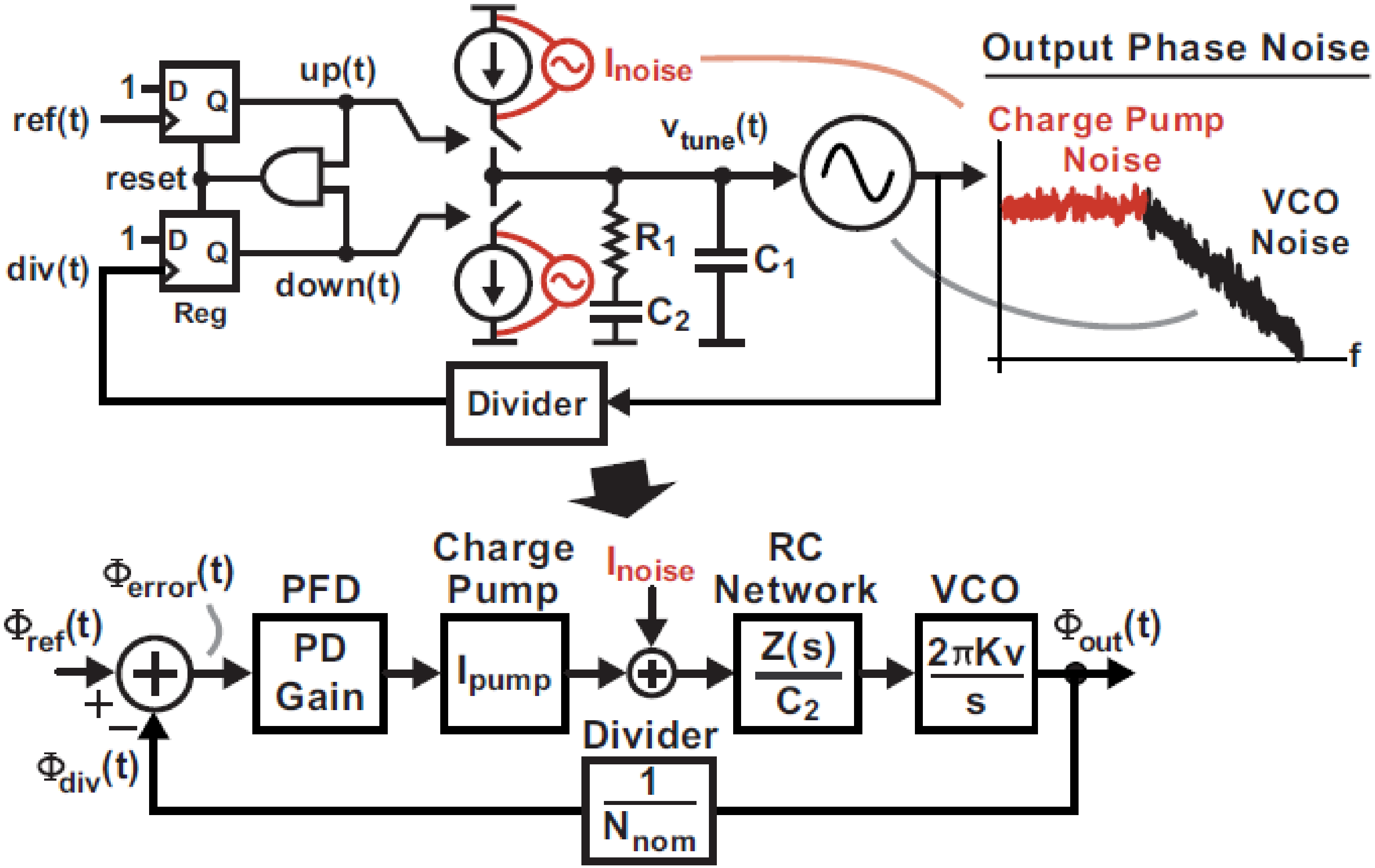
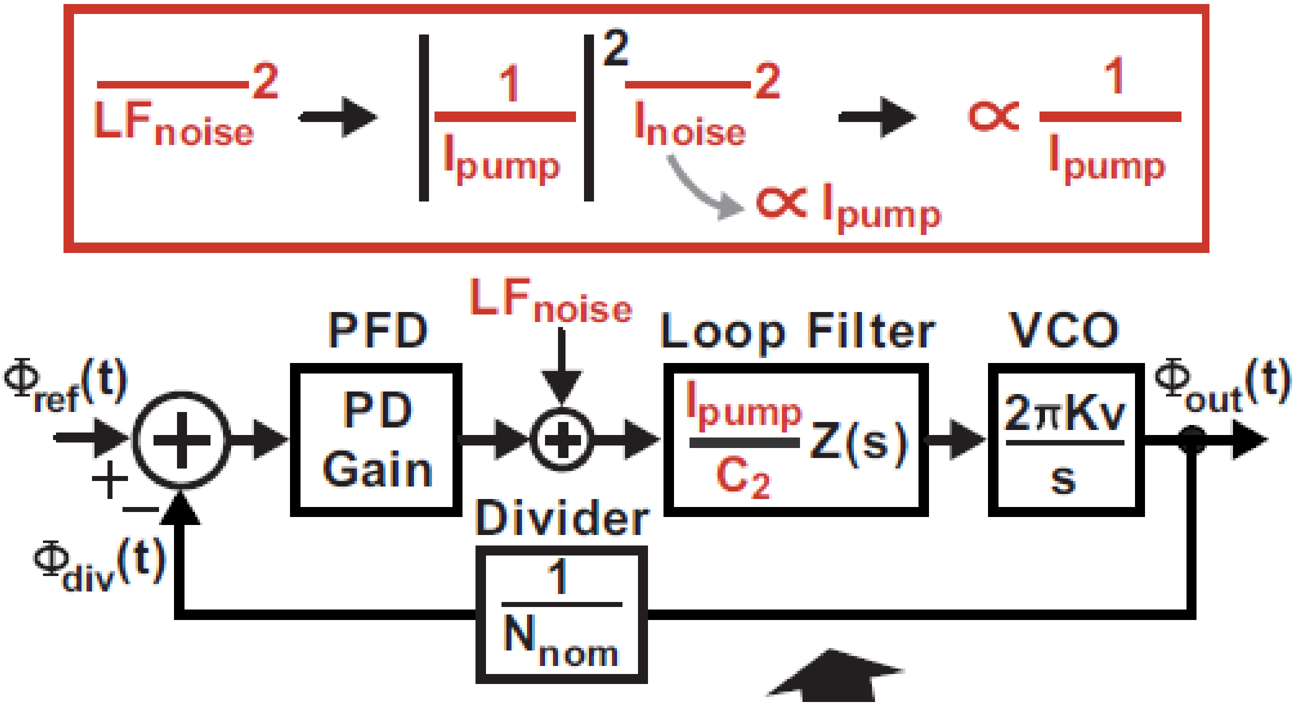
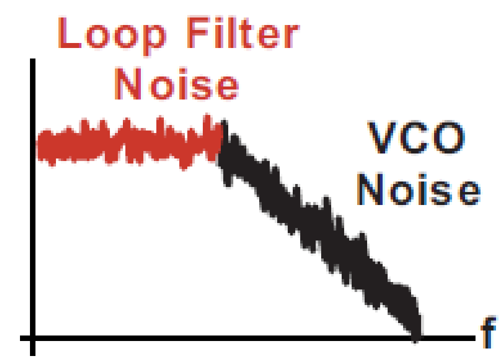
PLL Noise Analysis (I)



IEEE JSSC, pp. 2566-, Dec. 2010

PLL Noise Analysis (II)



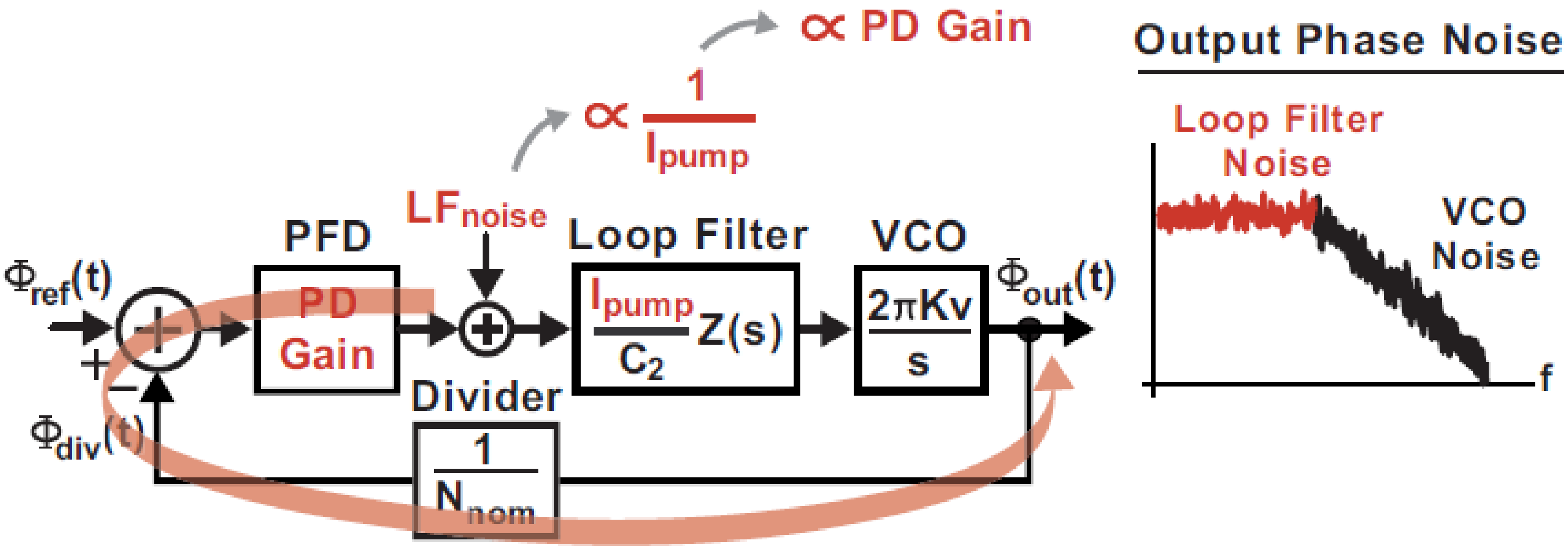


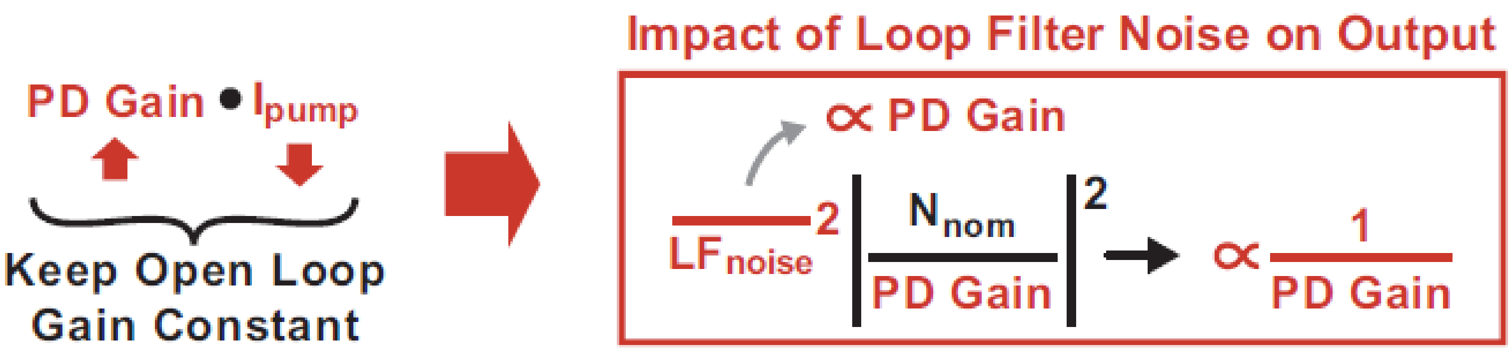
Increasing I_{pump} reduces Input-Referred Loop Filter Noise, but Open Loop Gain increases.

Area gets larger since C2 is typically increased to maintain desired open loop gain

IEEE JSSC, pp. 2566-, Dec. 2010

PLL Noise Analysis (III)

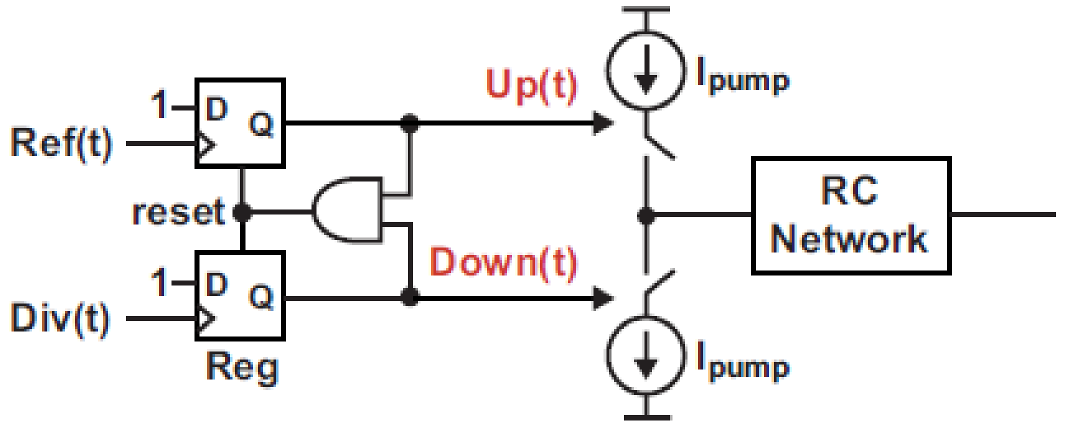


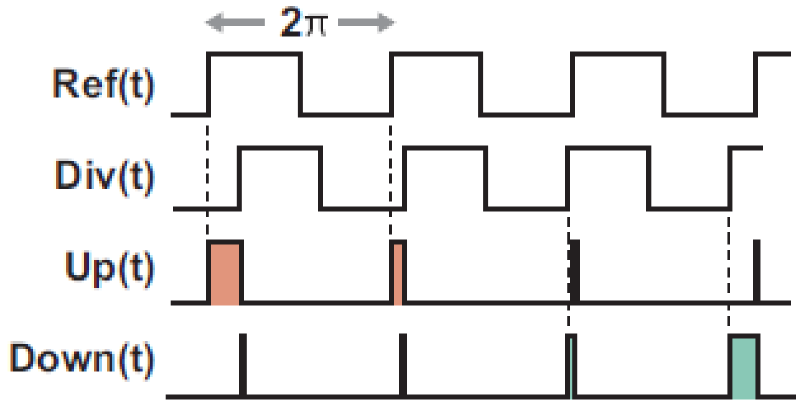


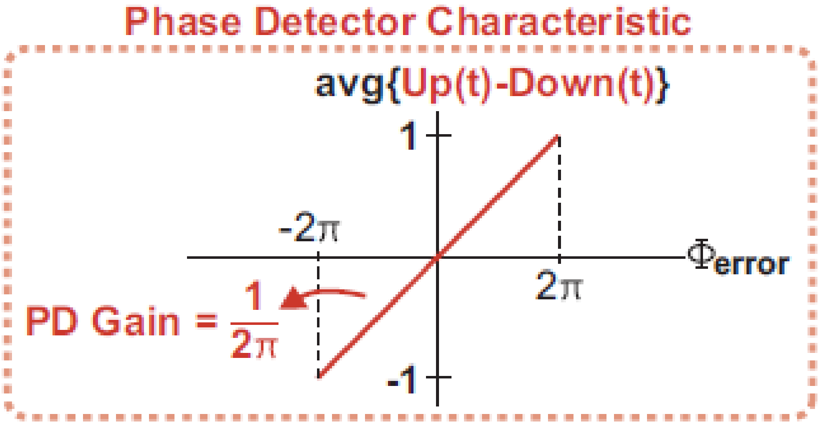
But how do we increase the PD gain?

IEEE JSSC, pp. 2566-, Dec. 2010

Phase Gain of a Classical Tristate PFD

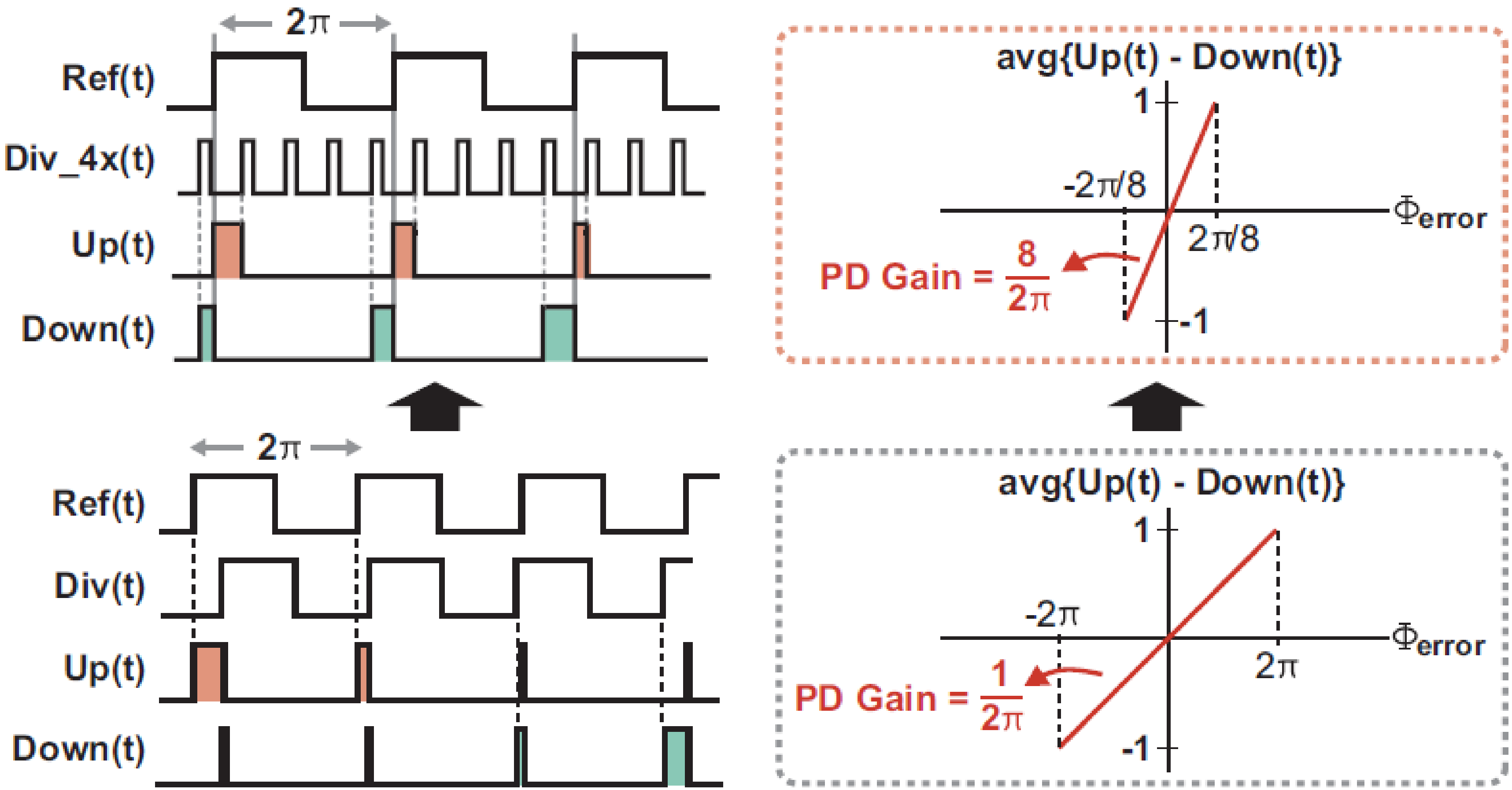






IEEE JSSC, pp. 2566-, Dec. 2010

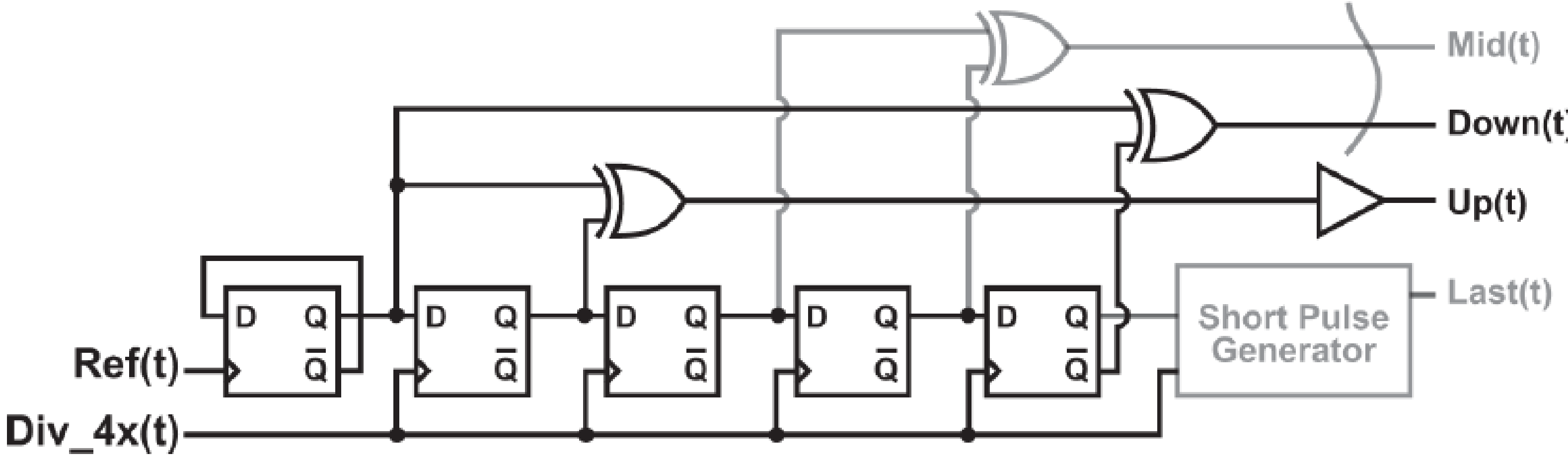
High Gain Phase Detector

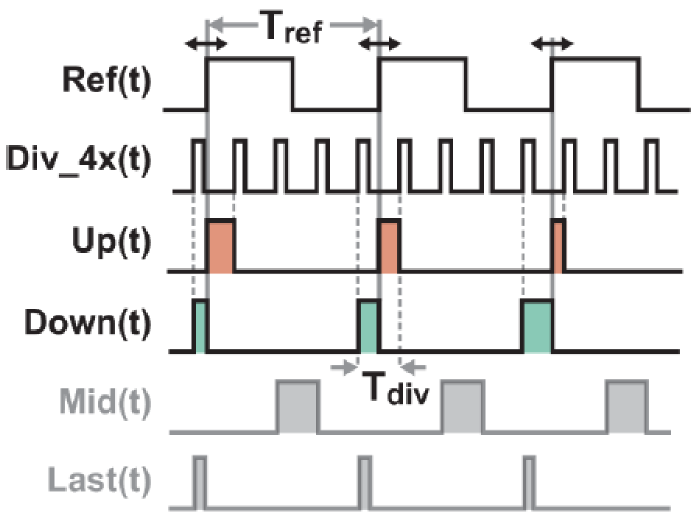


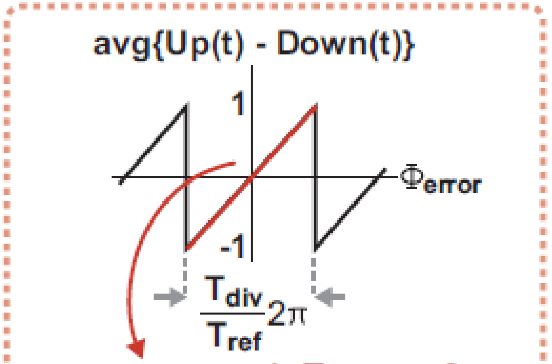
- **Reduce phase detection range to 1/4 of the Ref period**
  - **Achieves 8X increase in phase detector gain**

IEEE JSSC, pp. 2566-, Dec. 2010

A High-Gain PFD



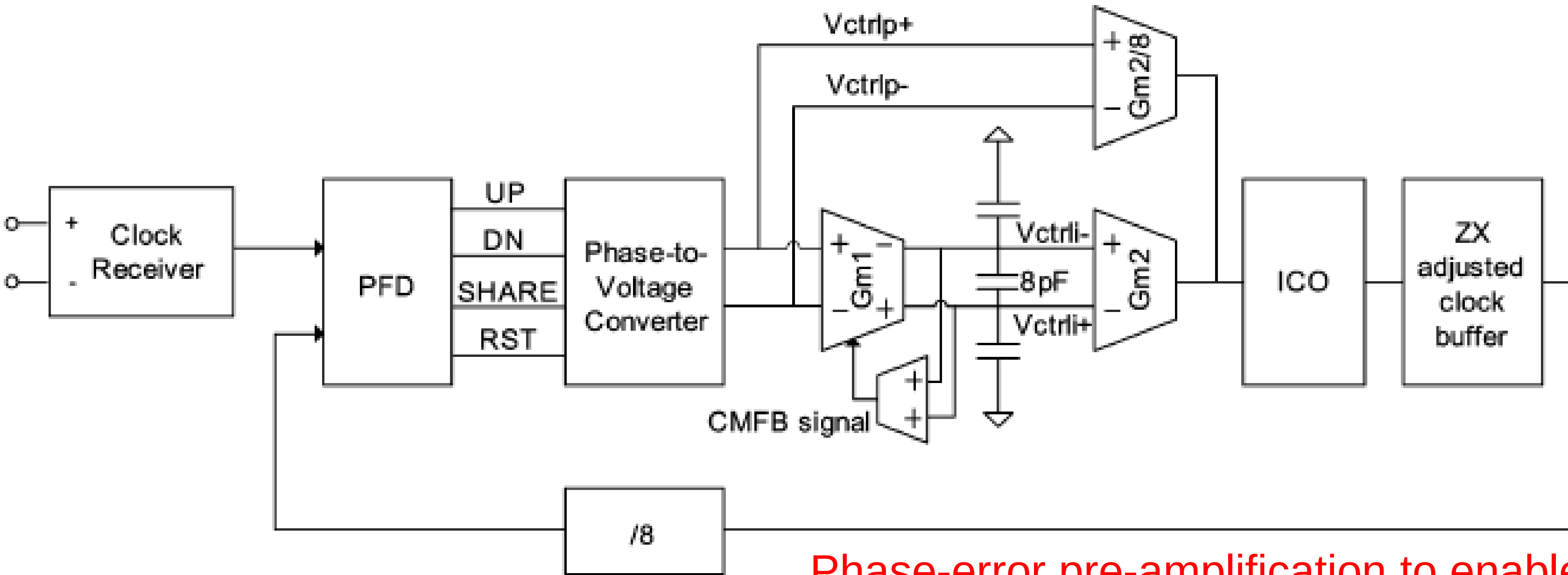




$$\text{PD Gain} = \frac{1}{2\pi}\frac{T_{ref}}{T_{div}}2 = \frac{8}{2\pi}$$

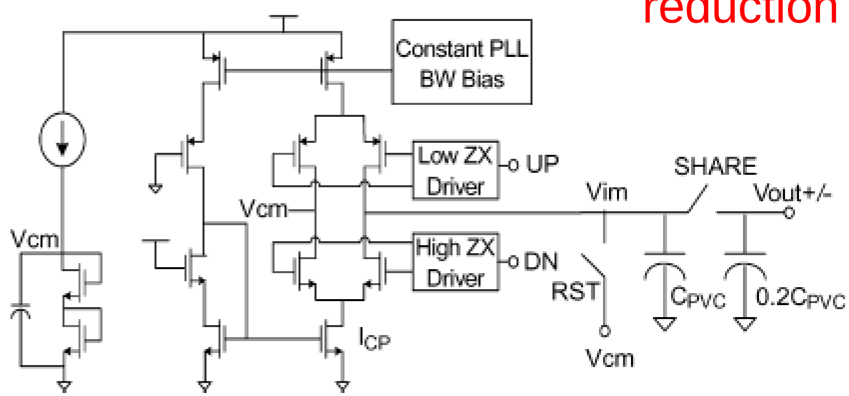
IEEE JSSC, pp. 2566-, Dec. 2010

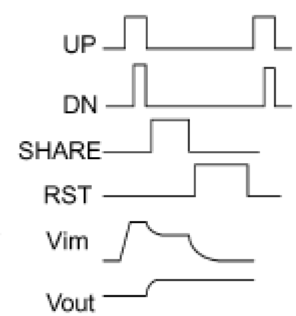
Phase-to-Voltage Converter



Phase-error pre-amplification to enable reduction of PLL in-band phase noise floor

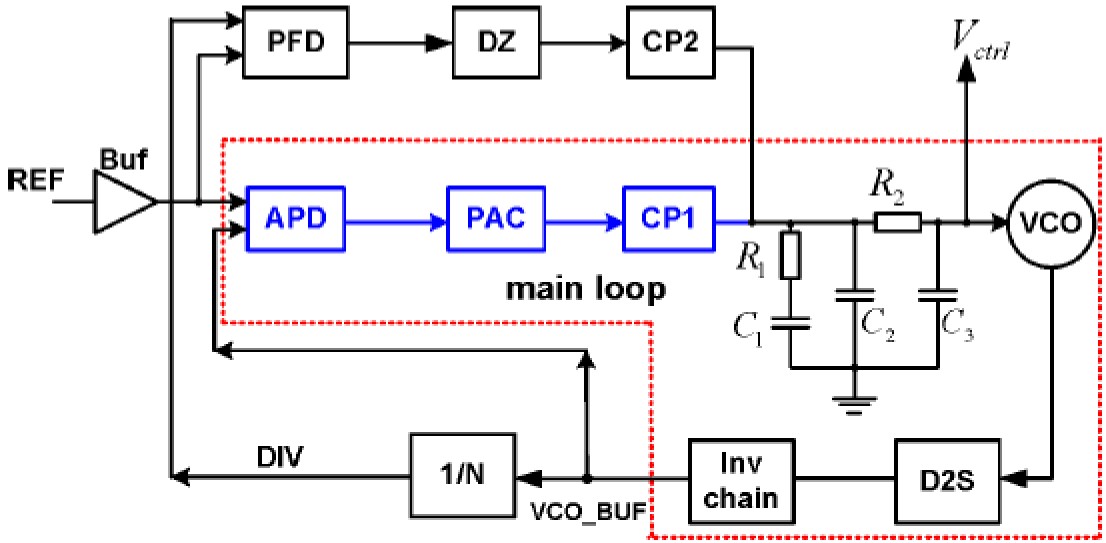
(Fully differential, one side shown)



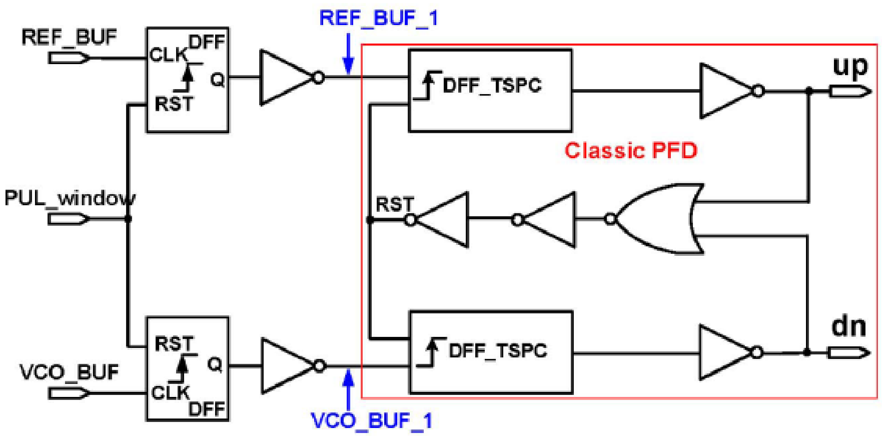


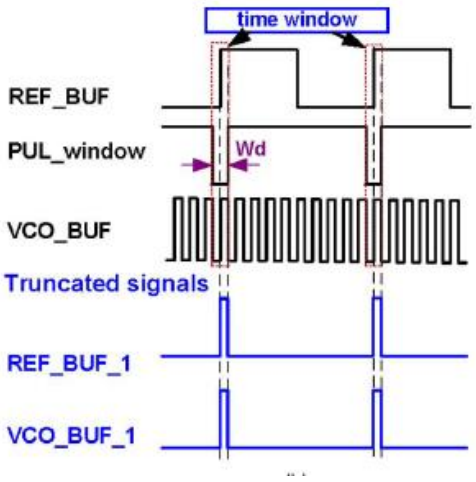
IEEE JSSC, pp. 2079-, Sept. 2008

Aperture Phase Detector



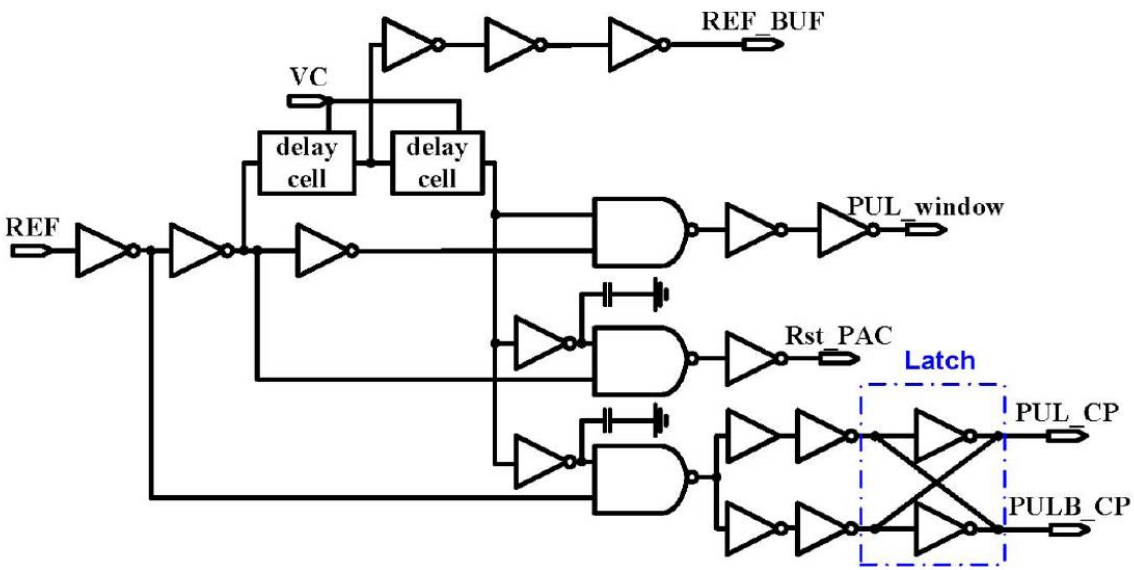
Aperture Phase Detector



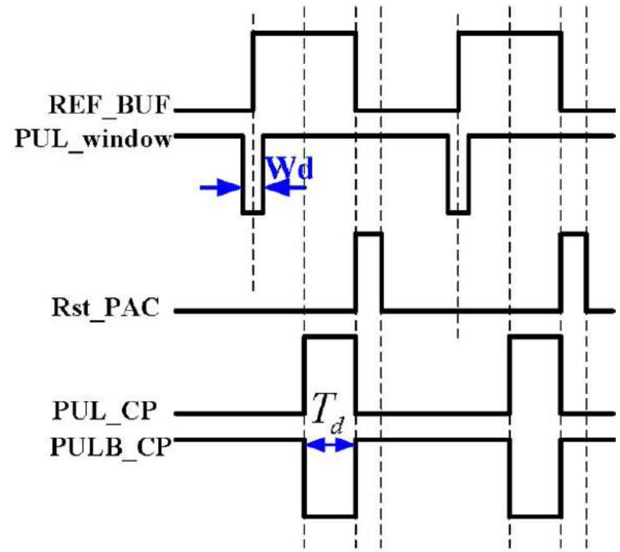


IEEE TCAS-I, pp. 37-, Jan. 2013

Phase-to-Analog Converter

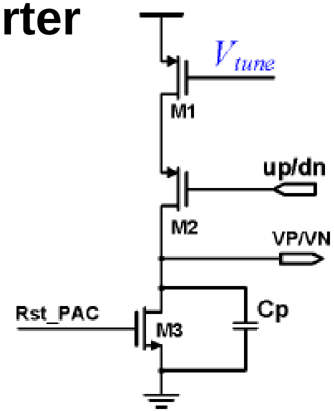


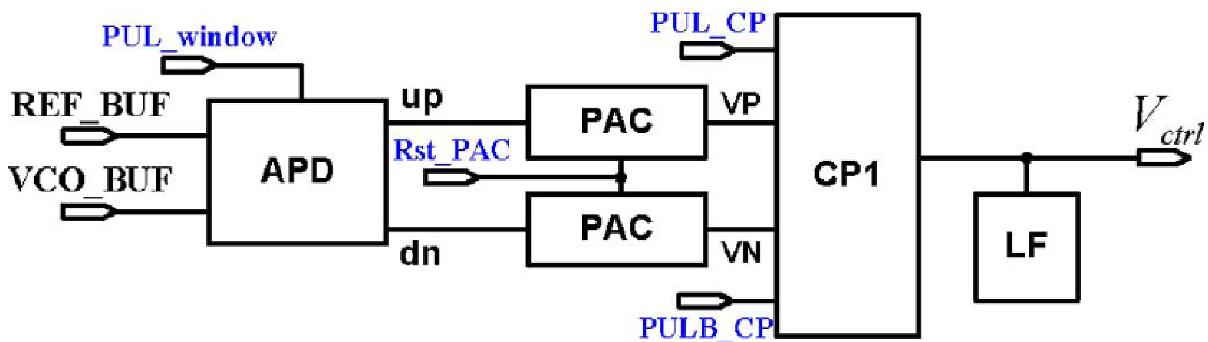
(a)



(b)

Phase-to-Analog Converter



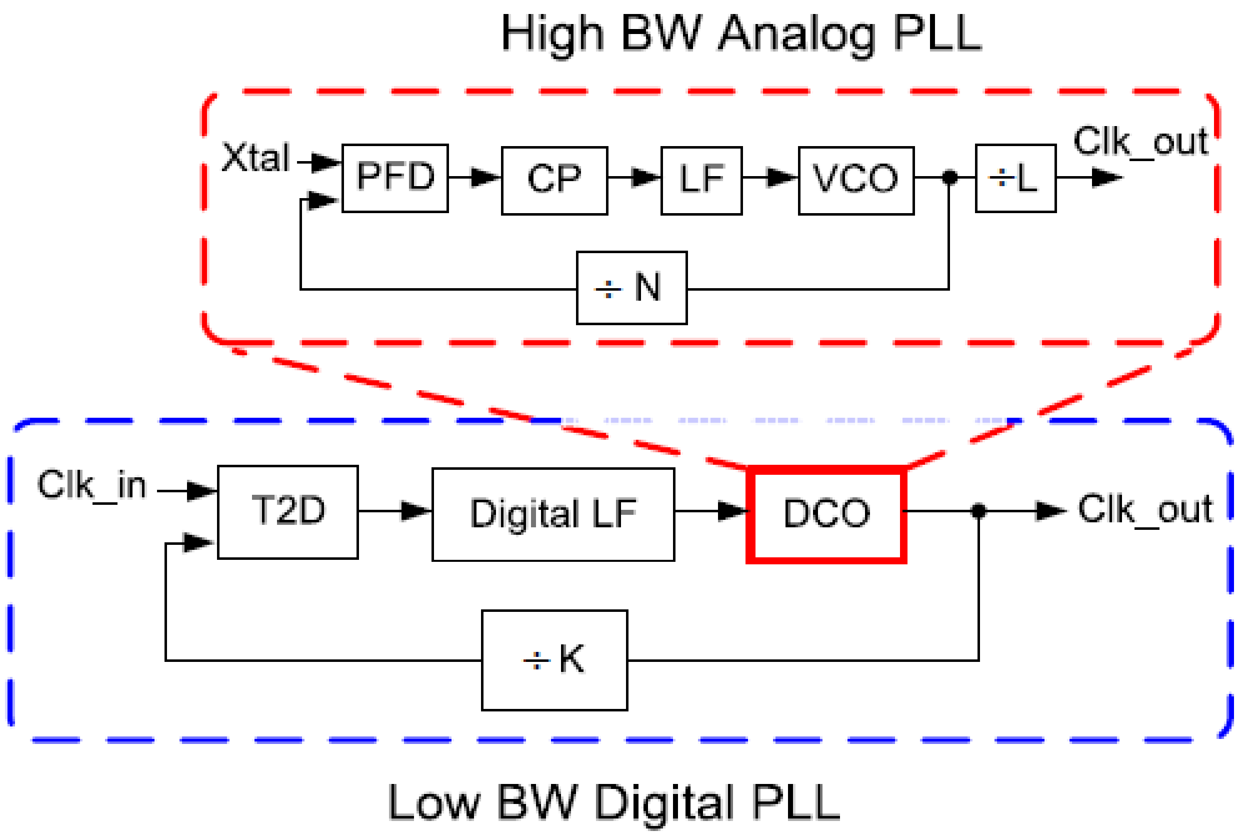


Low Noise PLLs

Several solutions

- Multiplying Delay-Locked Loop
- Noise filter: embedded FIR filter
- Sub-harmonically Injection-locked Technique
- Sub-sampling PD
- High-gain PFD
- Dual-Loop Hybrid Architecture

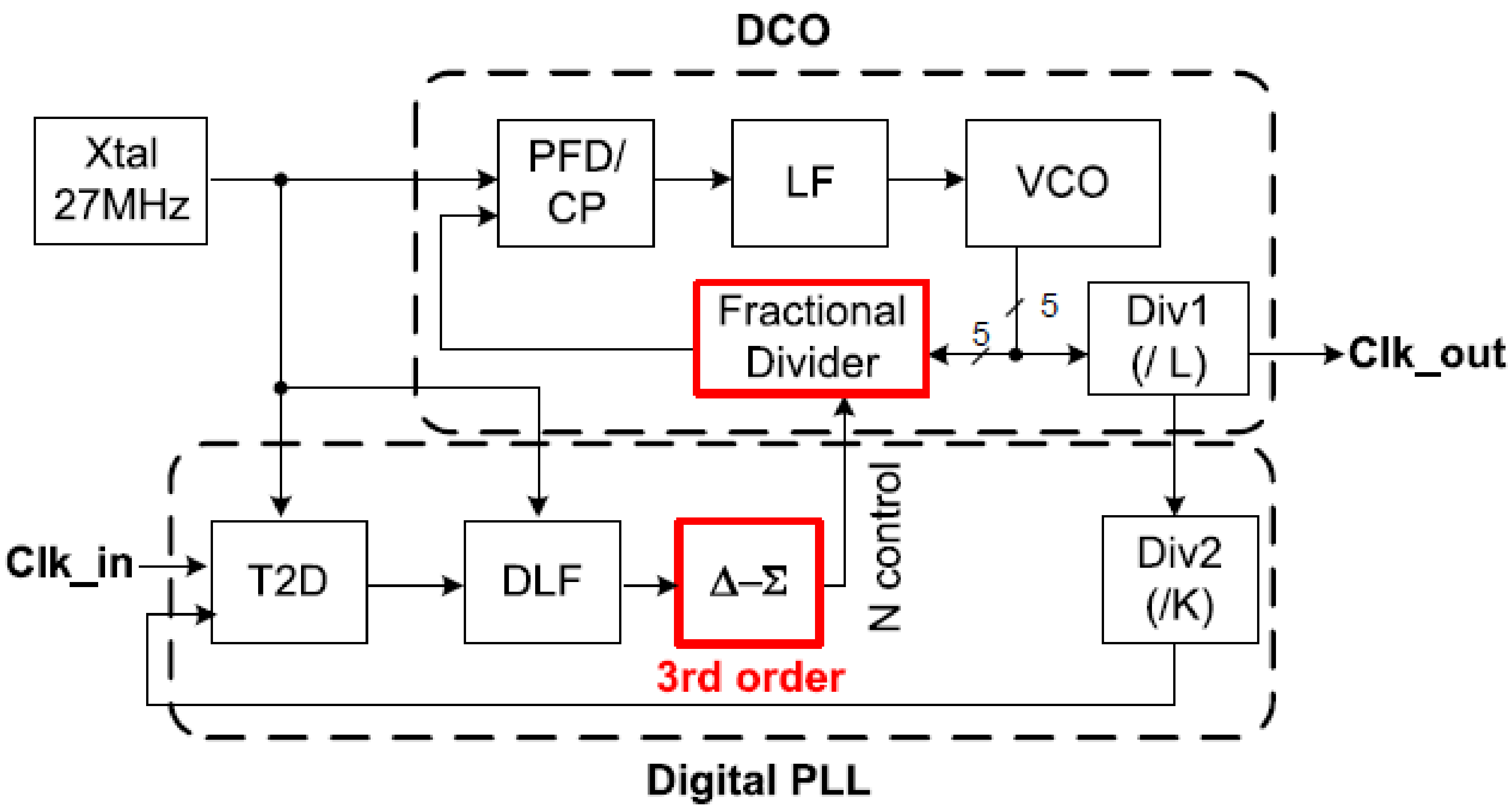
Dual-Loop Hybrid Architecture



- High BW analog PLL suppresses VCO noise
- Digital PLL achieves low BW with area efficient digital LF

ISSCC, Feb. 2006

Detail Circuit Block Diagram

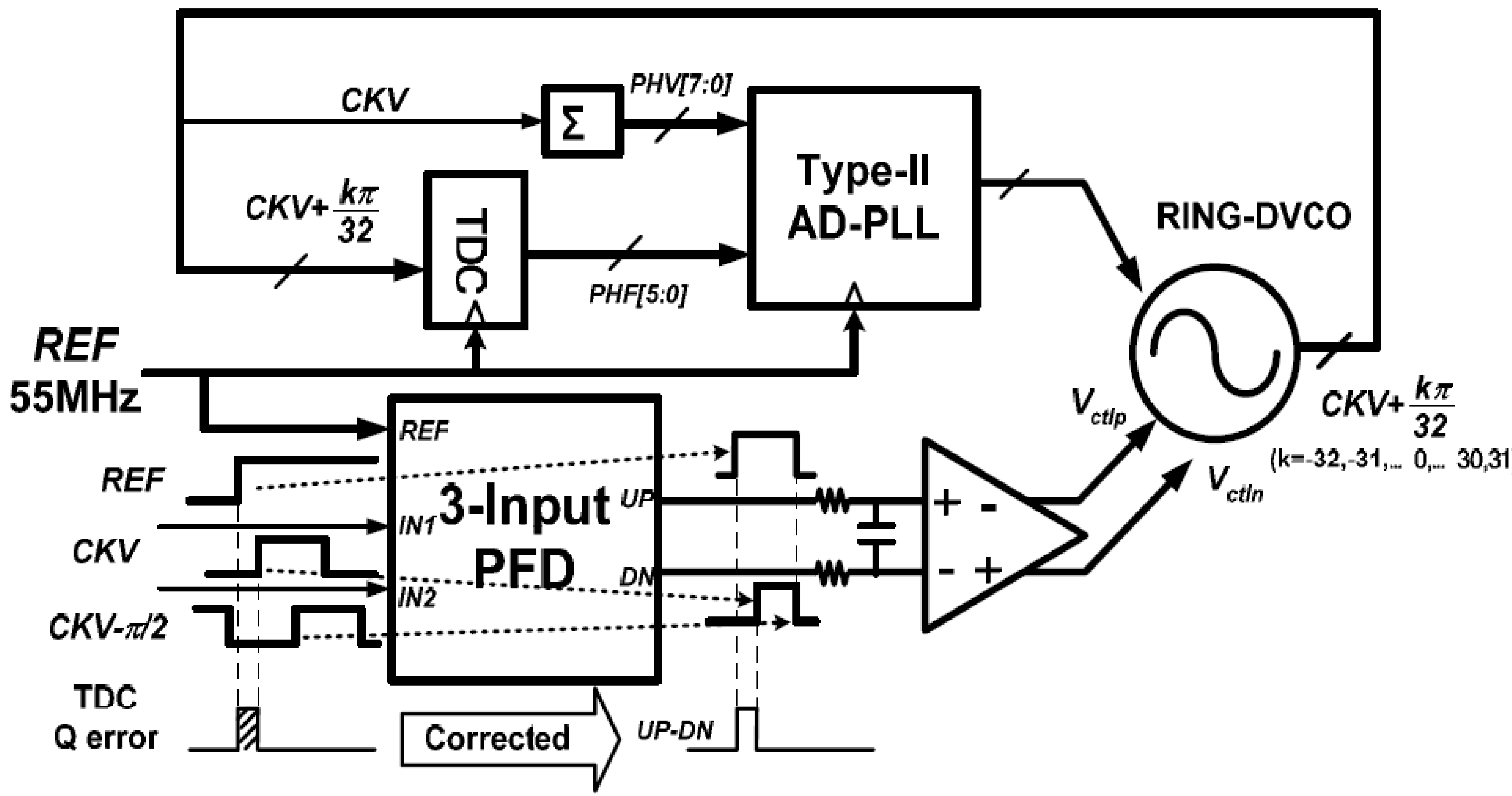


Limited digital code ⇒ Low frequency resolution

Δ-Σ modulator + fractional divider ⇒ fine resolution

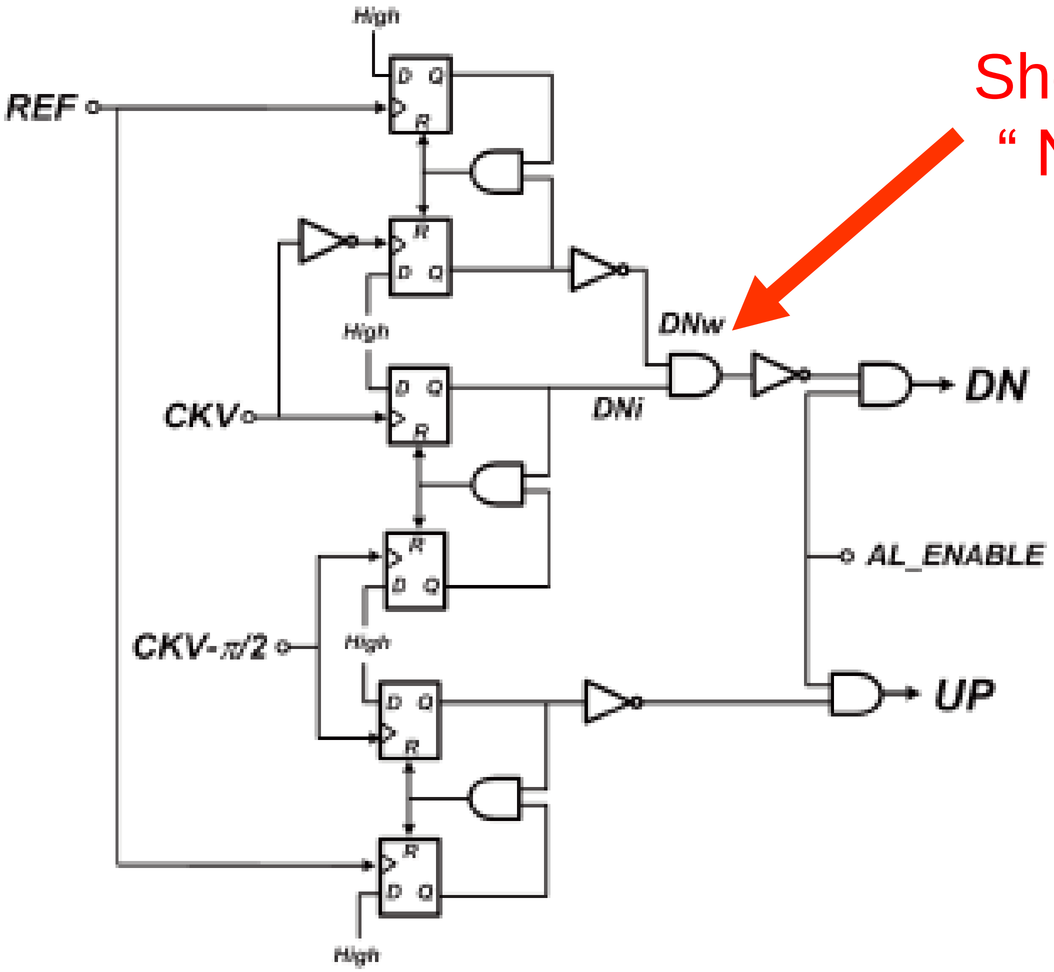
ISSCC, Feb. 2006

Hybrid PLL Architecture

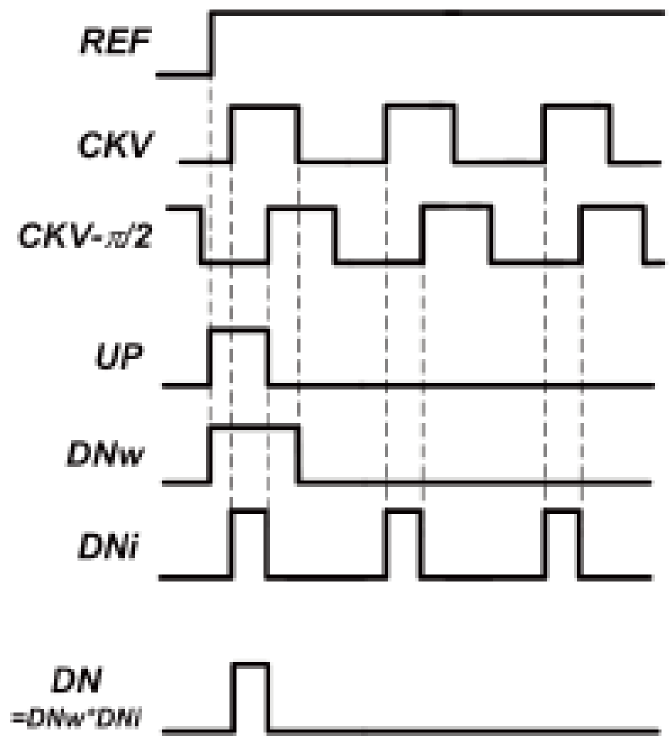


ISSCC, pp. 98-. Feb. 2011

Thee-input PFD



Should be
“ NAND”



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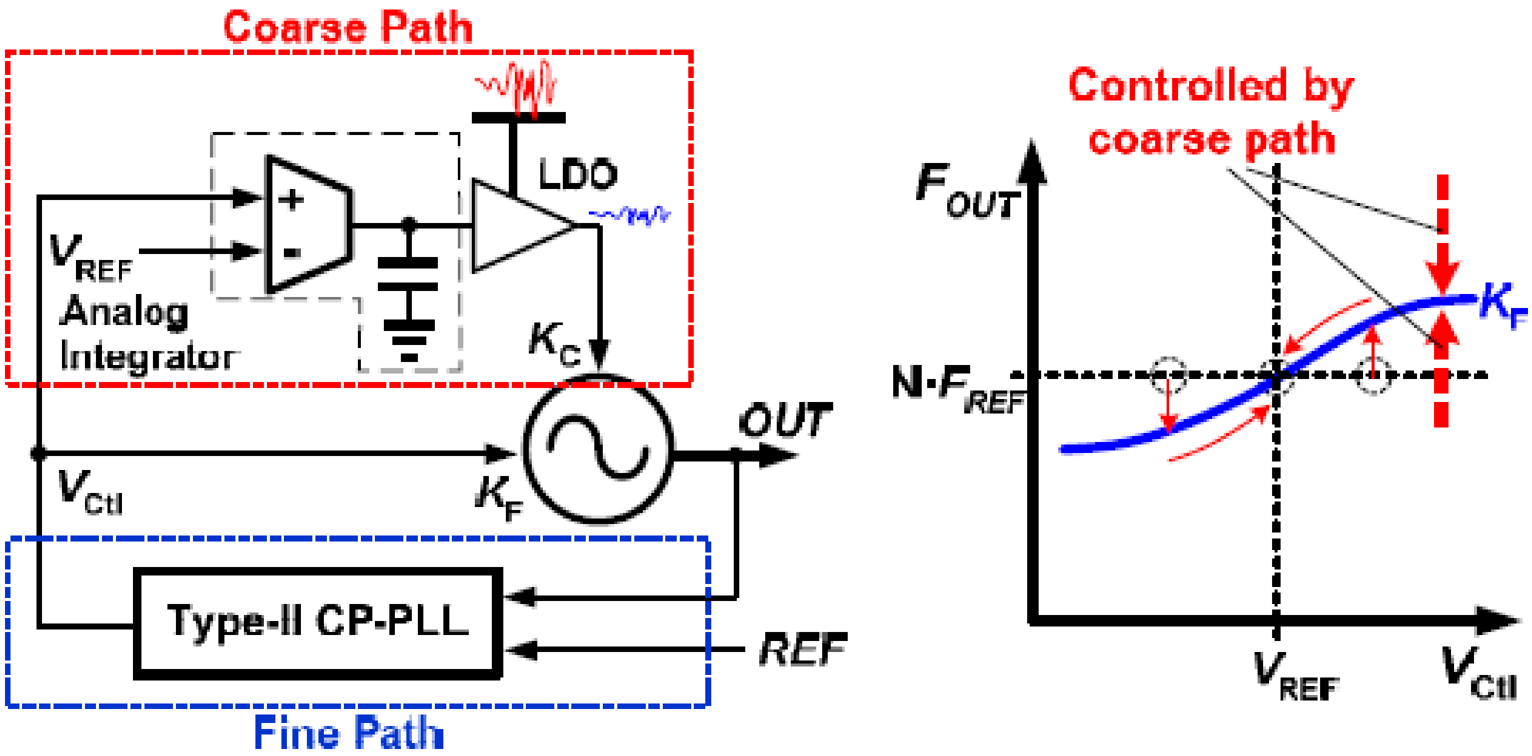
Dual-Tuning Architecture (I)



Pros: CP/LPF noise can be suppressed by integrator and lowering fine-path gain K_F. Coarse path achieves wide tracking range.

Cons: Limitation of lowering K_F because of stability.

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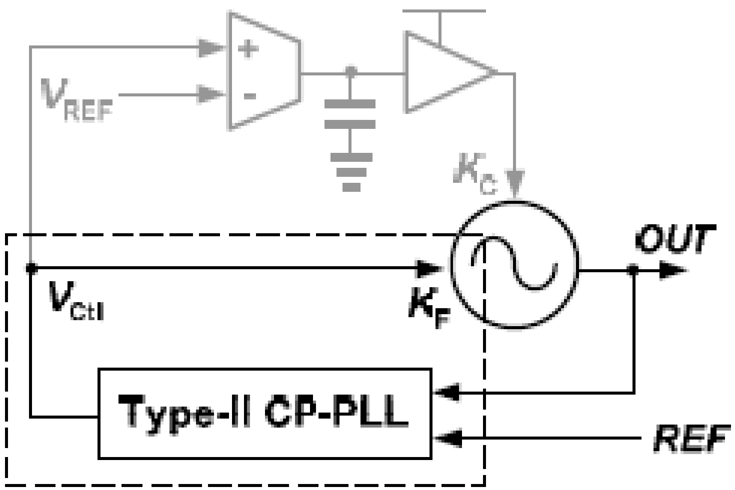
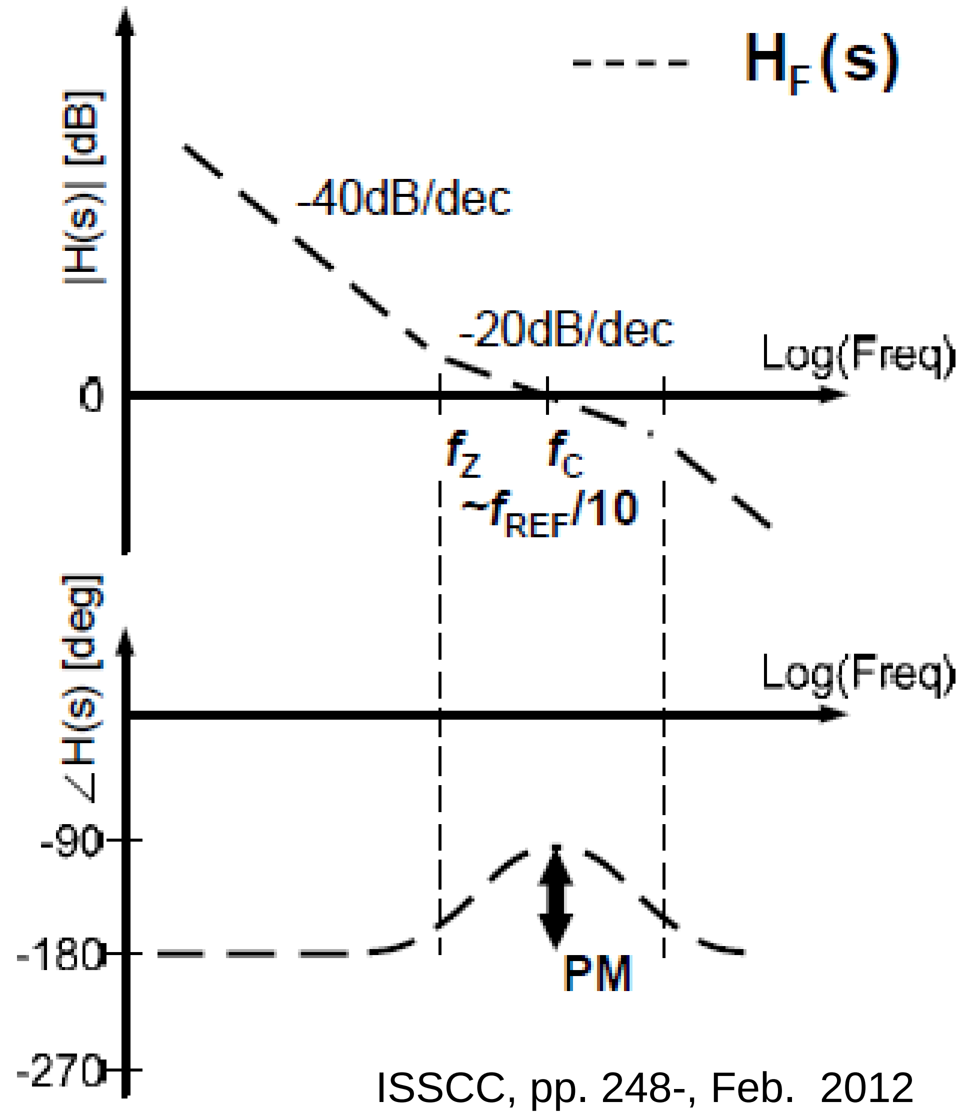
Dual-Tuning Architecture (II)





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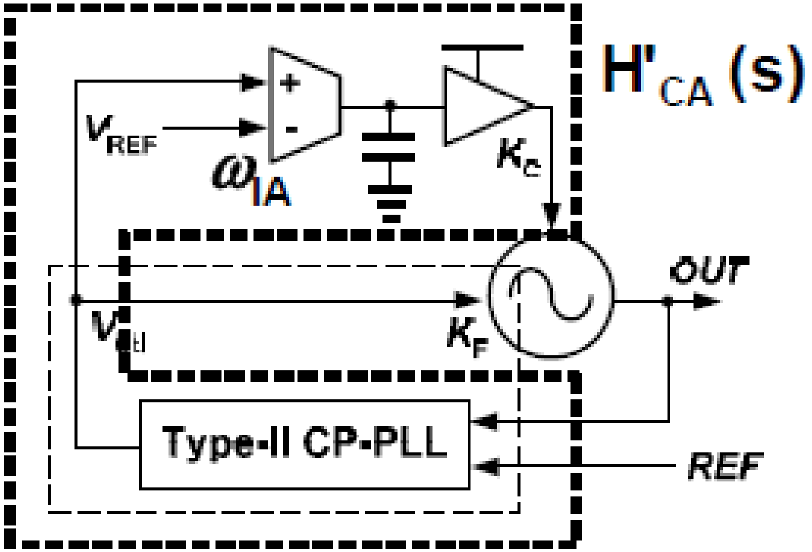
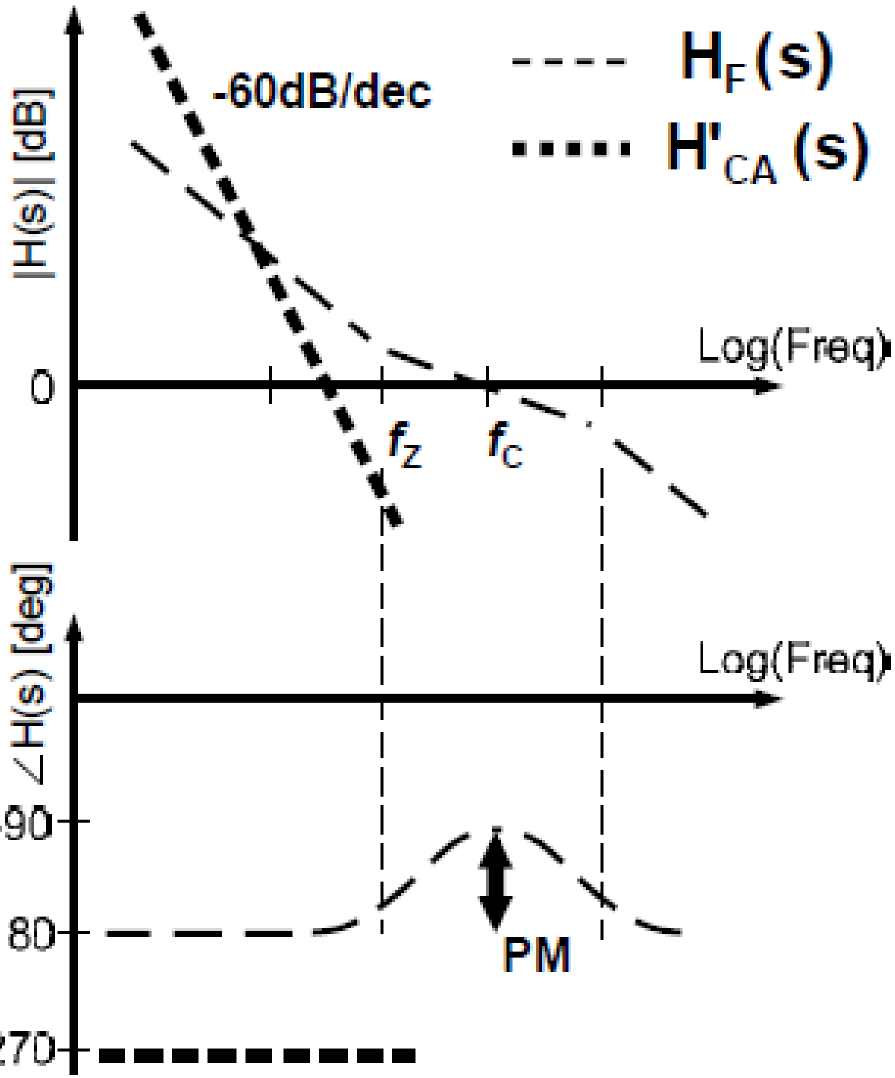
Dual-Tuning Architecture (III)



$$H(s) = H_F(s) + H'_{CA}(s)$$

$$= H_F(s) + \frac{H_F(s)}{K_F} H_{CA}(s)$$

$$\left(H_{CA}(s) = \frac{\omega_{IA} \cdot K_C}{s} \right)$$



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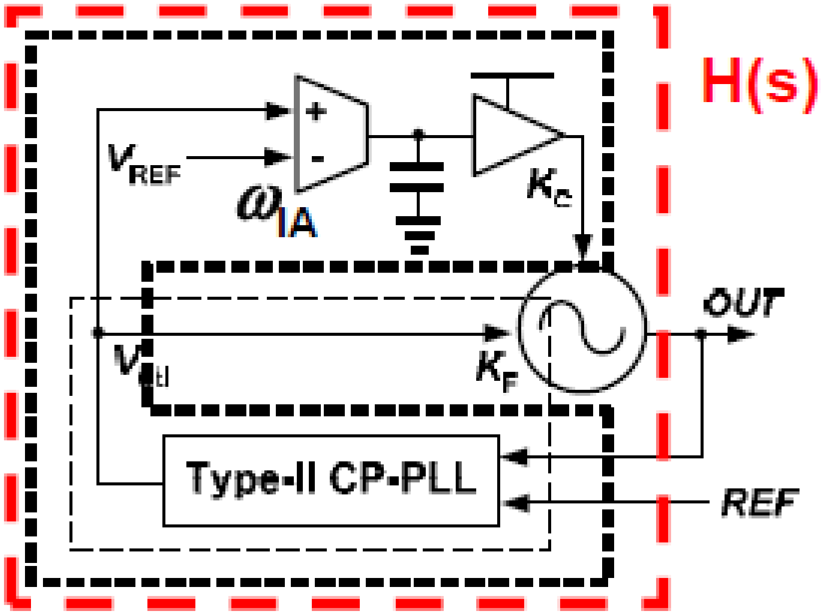
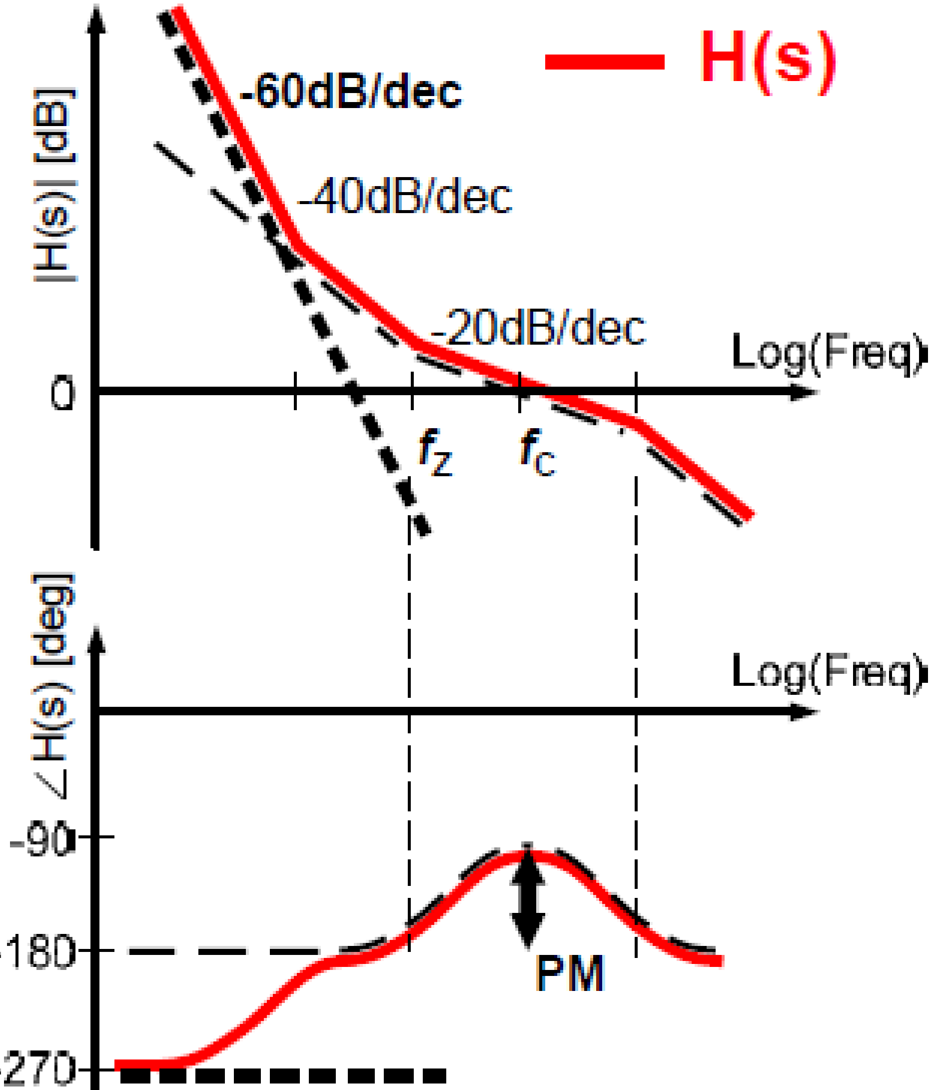
Dual-Tuning Architecture (IV)





$$H(s) = H_F(s) \cdot \underline{\left(\frac{s + \omega_{IA}(K_C/K_F)}{s} \right)}$$

H(s) has three poles at origin. $\rightarrow$ **Type-III**

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Design Constraint for Sufficient Stability

Our design has

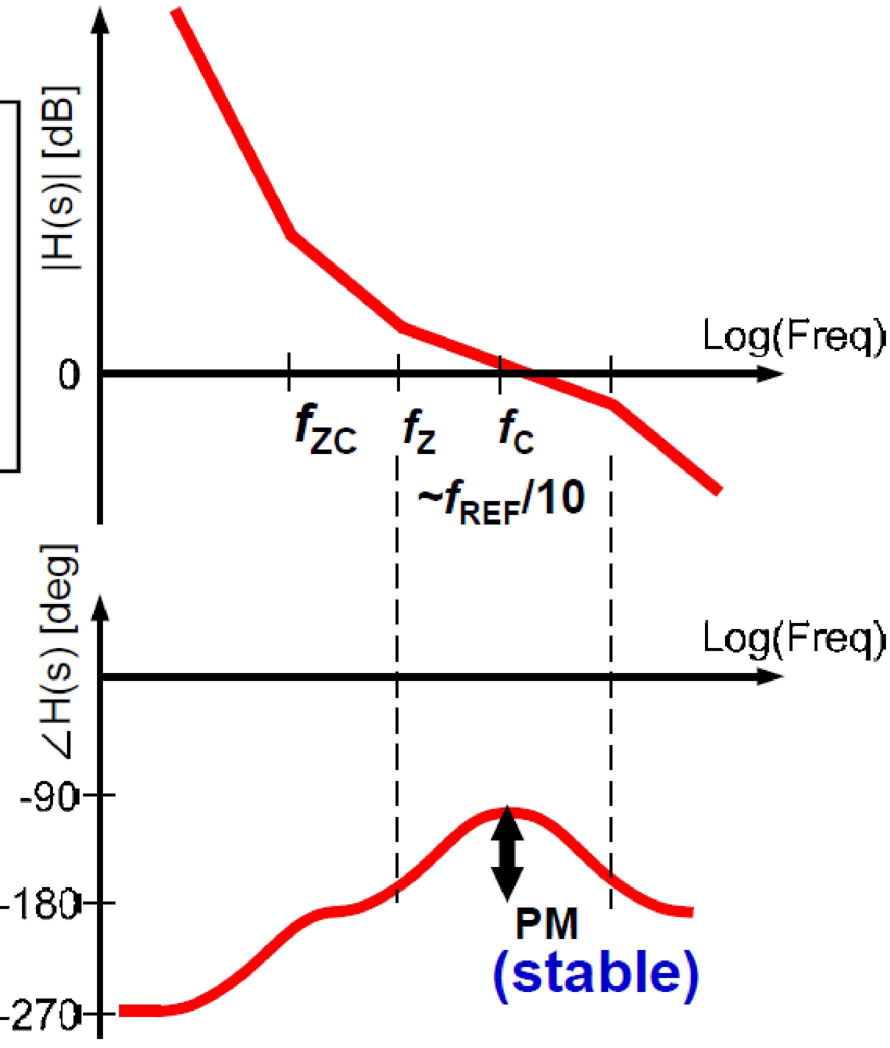
K_C = 10GHz/V f_{REF} = 10MHz
f_c = 1MHz
f_z = 100kHz
$f_{zc}= f_{IA}(K_C/K_F)$ **= 10kHz**
(for sufficient phase margin)

If K_F = 10MHz/V,

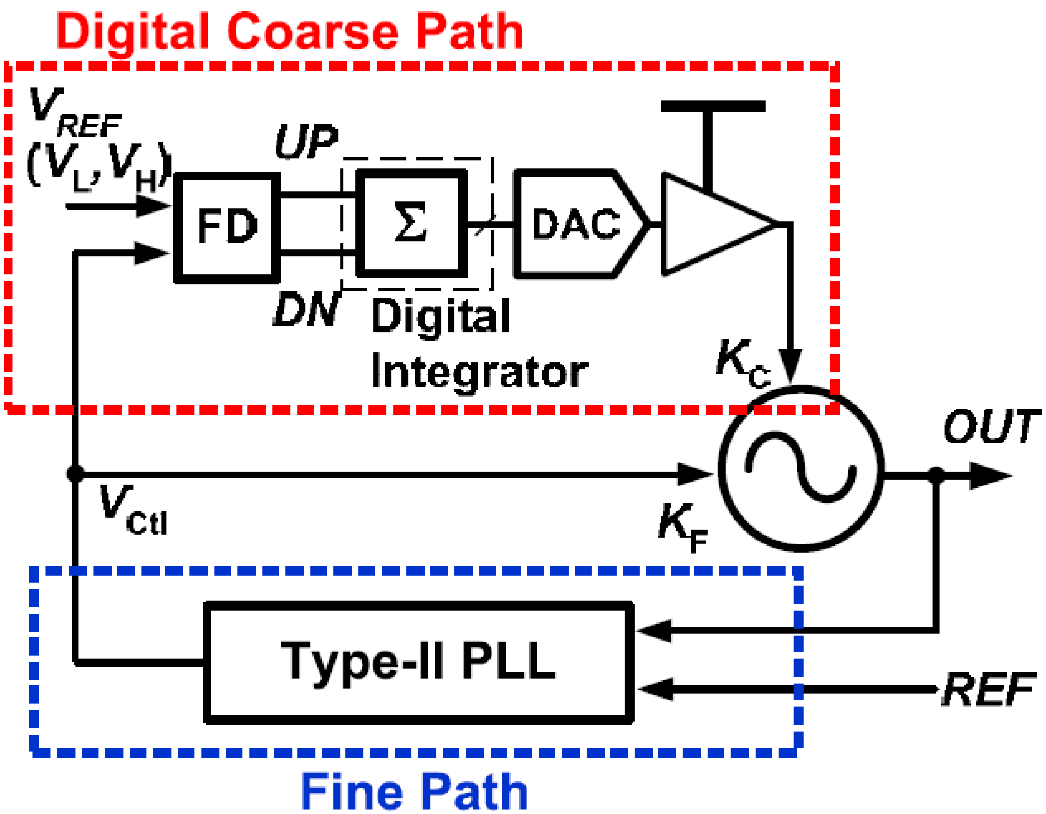
f_{IA} must be set to **10Hz!!!**

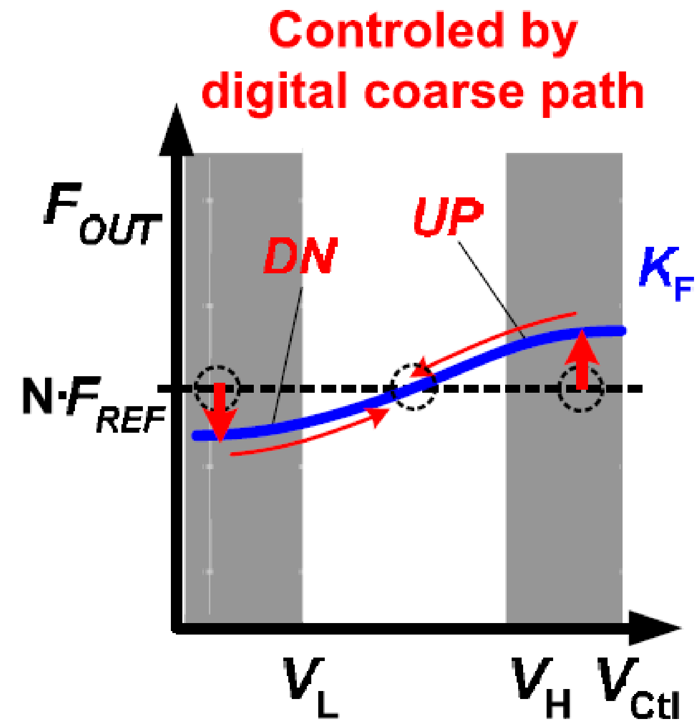
Quite tough for CMOS design

(e.g. **>1nF capacitor** for 1uS conventional Gm-C filter.)



Digitally Stabilized DT-PLL





- Digital coarse path greatly improves PLL stability.
- Coarse path always keeps V_{Ctl} between V_L and V_H.